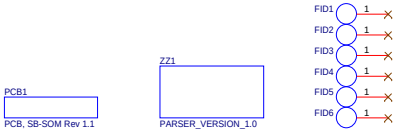
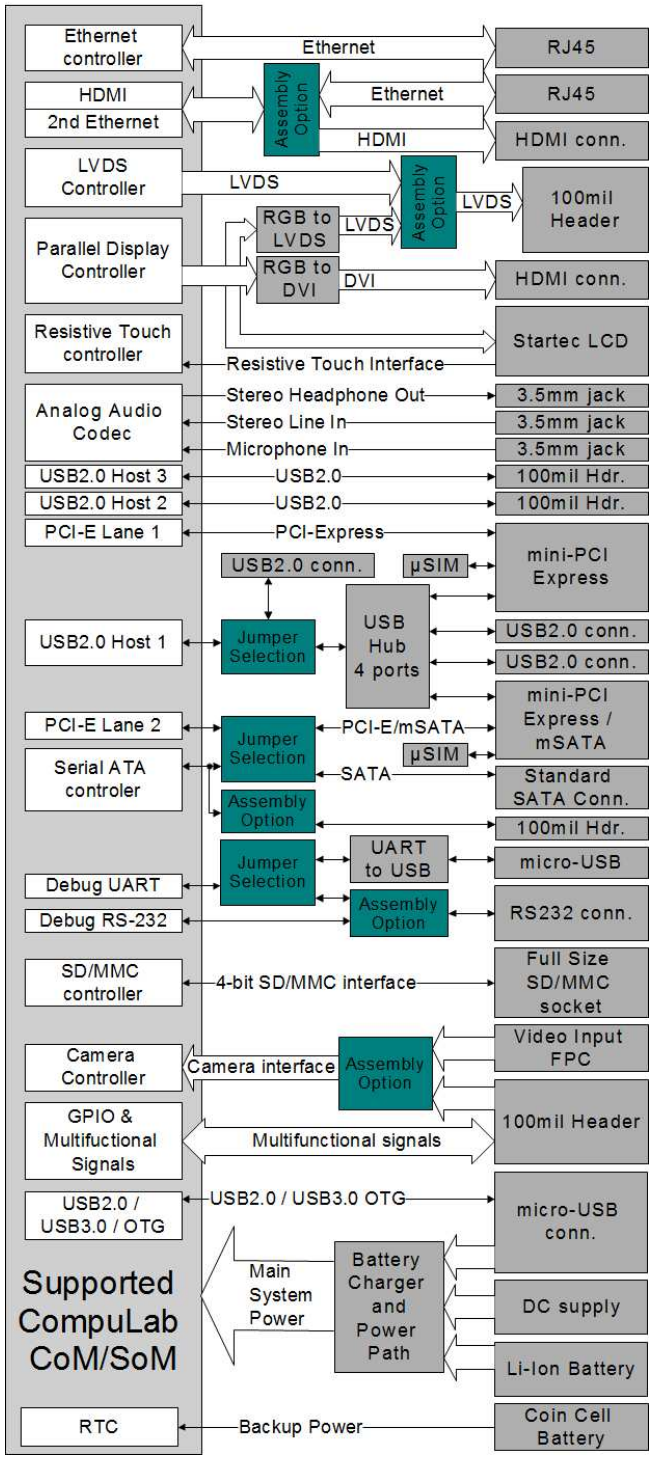
SB-SOM

BOARD REVISION: 1.1


```
CARRIER BOARD PRIMARY I2C BUS SLAVES (7bit address):
--------------------------------------------------------------------
0b010,0000 - Carrier GPIO Expander
0b011,0110 - DS2786 Battery Supervisor
0b011,1001 - DVI Transmitter
0b101,0100..0b1010111 - Carrier ID EEPROM (except SB-SOM-T43)
0b101,0000..0b1010011 - Carrier ID EEPROM (SB-SOM-T43 only)
0b110,1011 - BQ24161 battery charger & power-path
0b110,1110 - PCI-E REFCLK fanout
```



SB-SOM rev1v1



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BOARD REVISION: 1.0

1. Initial Revision with support for the following SoMs:
1.1. CM-T43
1.2. CM-T54
1.3. CM-QS600

BOARD REVISION: 1.1

1. Power supply scheme changed to improve battery/usb powered system operation.
2. Added initial support for CL-SOM-iMX6UL board.
3. Added initial support for CL-SOM-AM57x board.
4. Board phyiscal dimensions increased to improve usability
5. Improved (silk) description of various board jumpers, buttons, LEDs and connectors.
6. Added production provisions
7. Added GPIO button to be used with CM-QS600
8. Improved backlight driver circuitry
9. Added pads for solderable spacers to comply with new SOM mechanical requirements
10. Removed obsolete PCIe spacers, replaced some with simple mechanical holes

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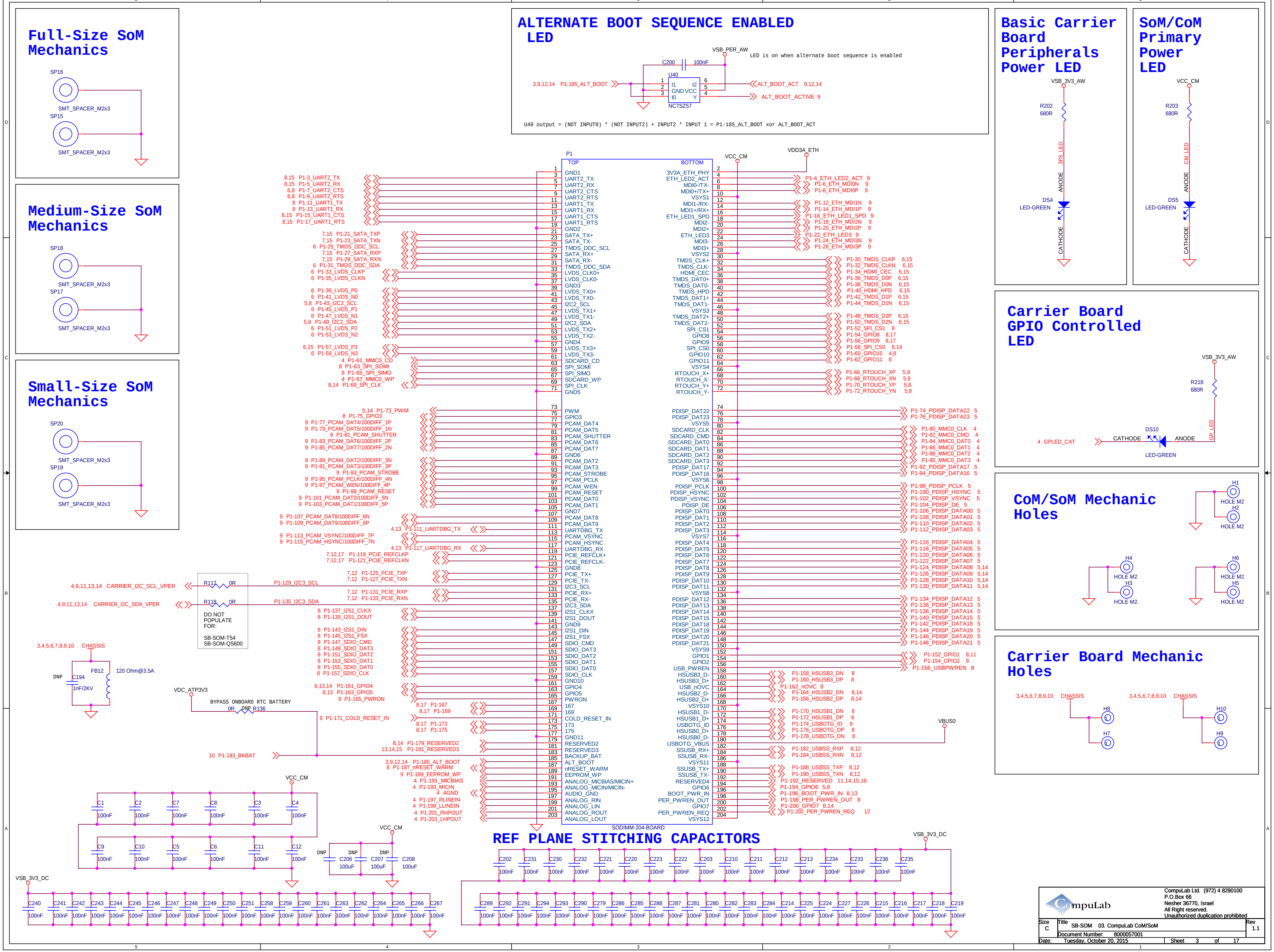

Full-Size SoM Mechanics
Medium-Size SoM Mechanics
Small-Size SoM Mechanics
ALTERNATE BOOT SEQUENCE ENABLED LED
LED is on when alternate boot sequence is enabled
U40 output = (NOT INPUT0) * (NOT INPUT2) + INPUT2 * INPUT 1 = P1-185_ALT_BOOT xor ALT_BOOT_ACT
Basic Carrier Board Peripherals Power LED
SoM/CoM Primary Power LED
Carrier Board GPIO Controlled LED
CoM/SoM Mechanic Holes
Carrier Board Mechanic Holes
REF PLANE STITCHING CAPACITORS
BYPASS ONBOARD RTC BATTERY
DO NOT POPULATE FOR: SB-SOM-T54 SB-SOM-QS600
SODIMM-204-BOARD
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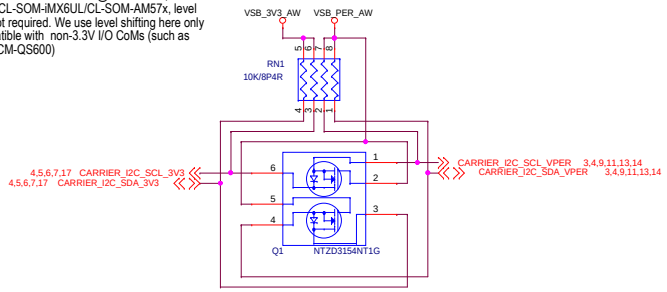
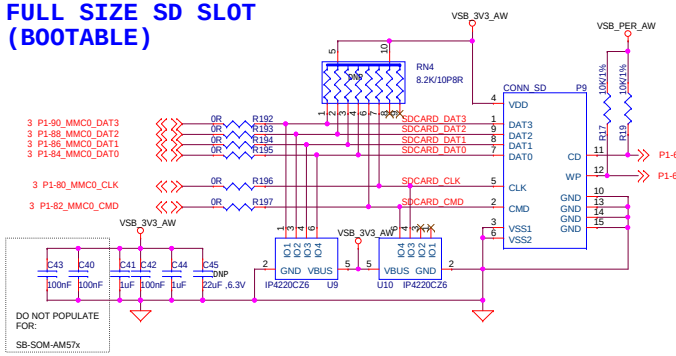
CARRIER BOARD PRIMARY I2C BUS LEVEL SHIFT

Circuitry is designed to shift
I2C signals logic levels between
VSB_PER (1.8 or 3.3V) and 3.3V.

NOTE: In case CoM/SoM I/O is @ 3.3V levels, such as CM-T43/CL-SOM-iMX6UL/CL-SOM-AM57x, level shifting is not required. We use level shifting here only to be compatible with non-3.3V I/O CoMs (such as CM-T54 or CM-QS600)

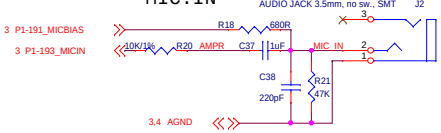


FULL SIZE SD SLOT (BOOTABLE)

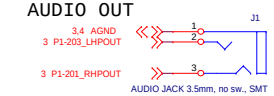


ANALOG AUDIO

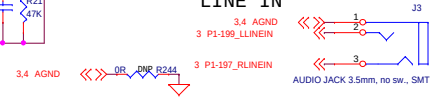
MIC.IN



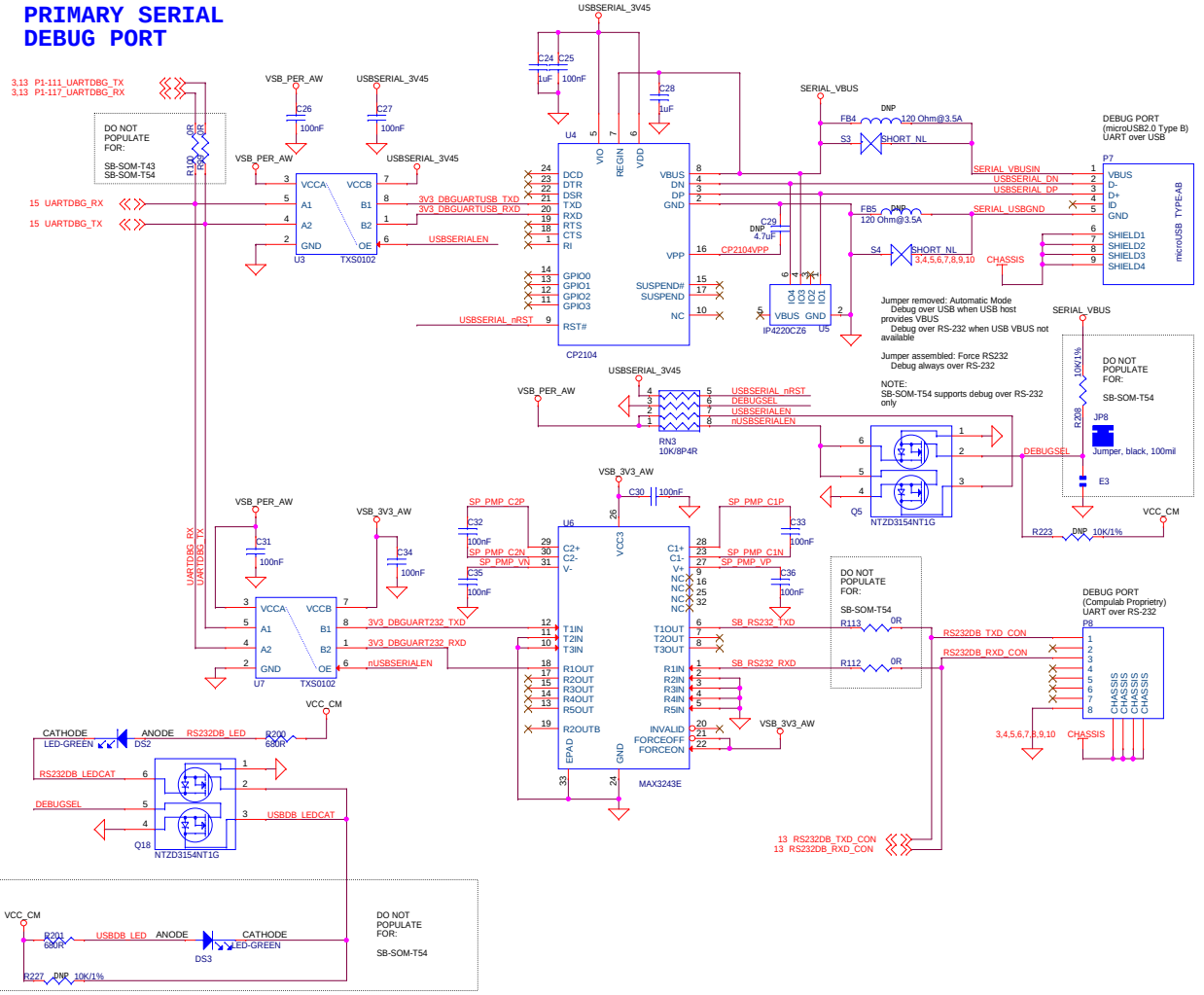
AUDIO OUT



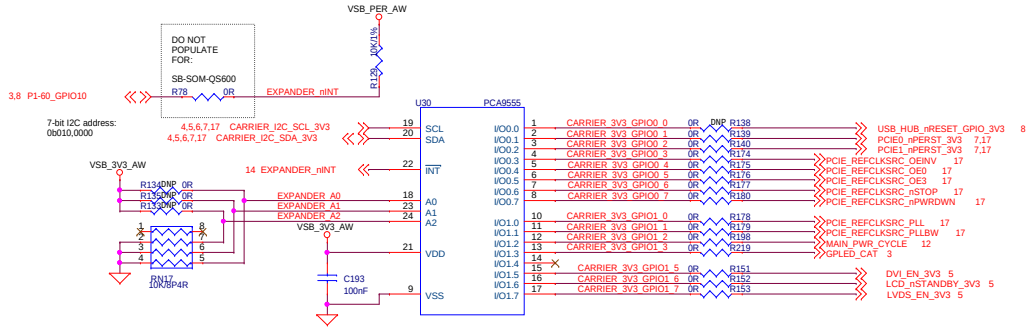
LINE IN



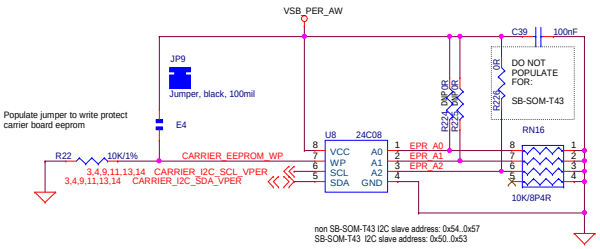
PRIMARY SERIAL DEBUG PORT



CARRIER GPIO EXPANDER



CARRIER BOARD EEPROM



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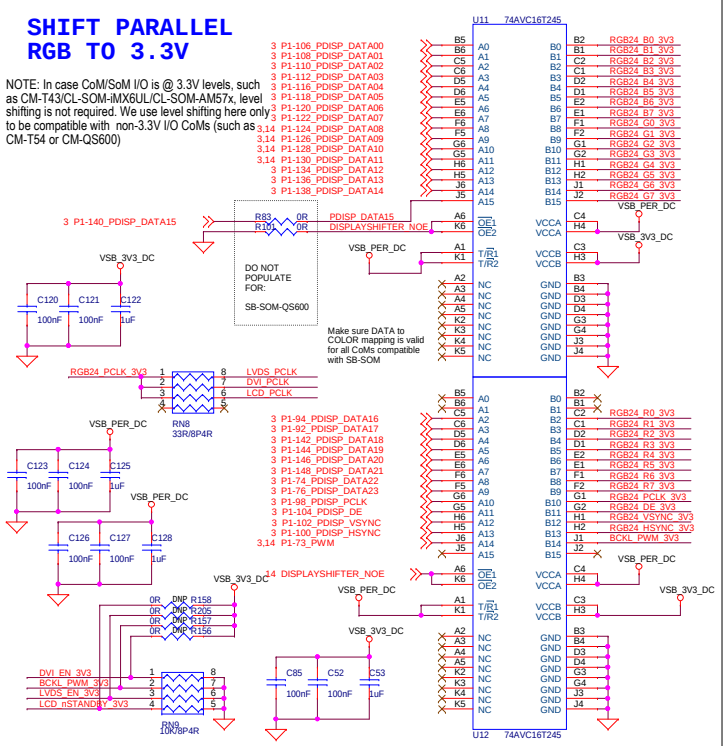
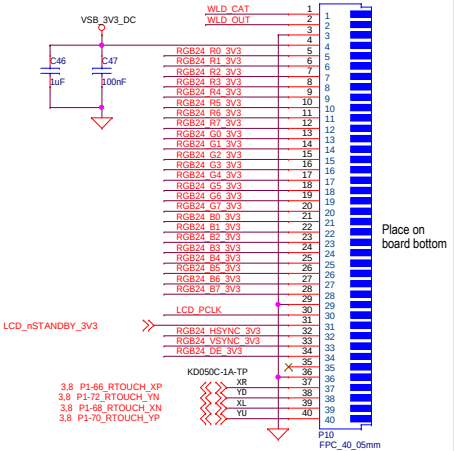
SHIFT PARALLEL RGB TO 3.3V

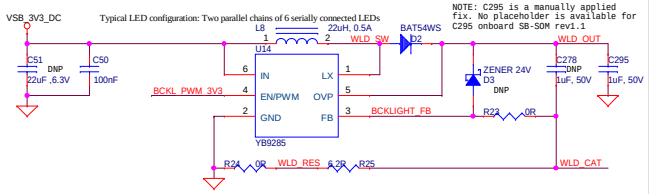
NOTE: In case CoM/SoM I/O is @ 3.3V levels, such as CM-T43/CL-SOM-iMX6UL/CL-SOM-AM57x, level shifting is not required. We use level shifting here only to be compatible with non-3.3V I/O CoMs (such as CM-T54 or CM-QS600)



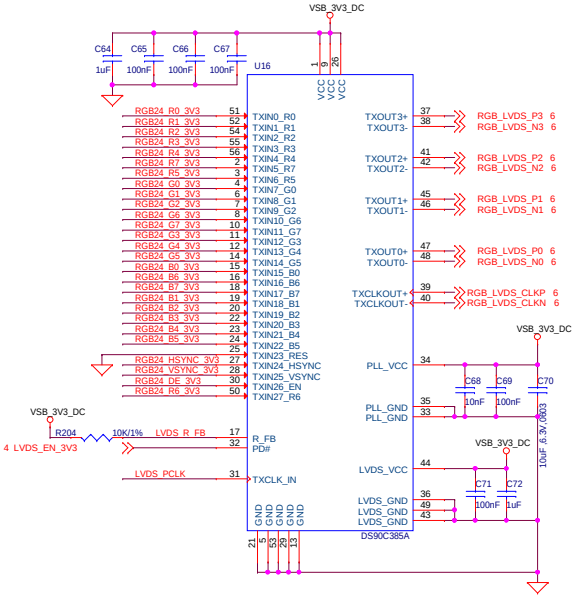
PARALLEL RGB LCD & TOUCH

SHENZHEN STARTEK ELECTRONIC TECHNOLOGY KD050C-1A-TP LCD

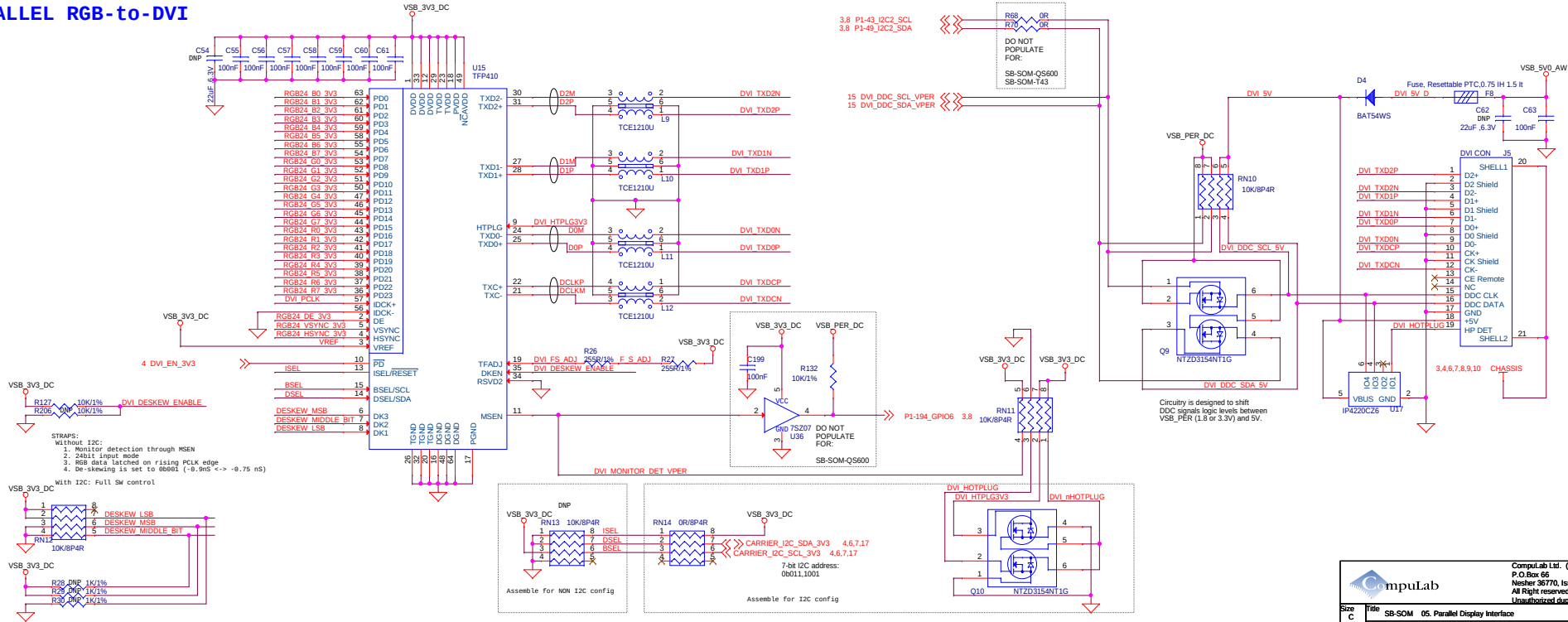




PARALLEL RGB to LVDS



PARALLEL RGB-to-DVI



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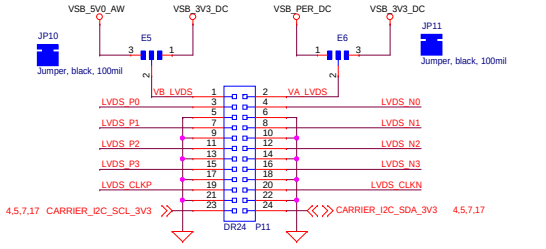
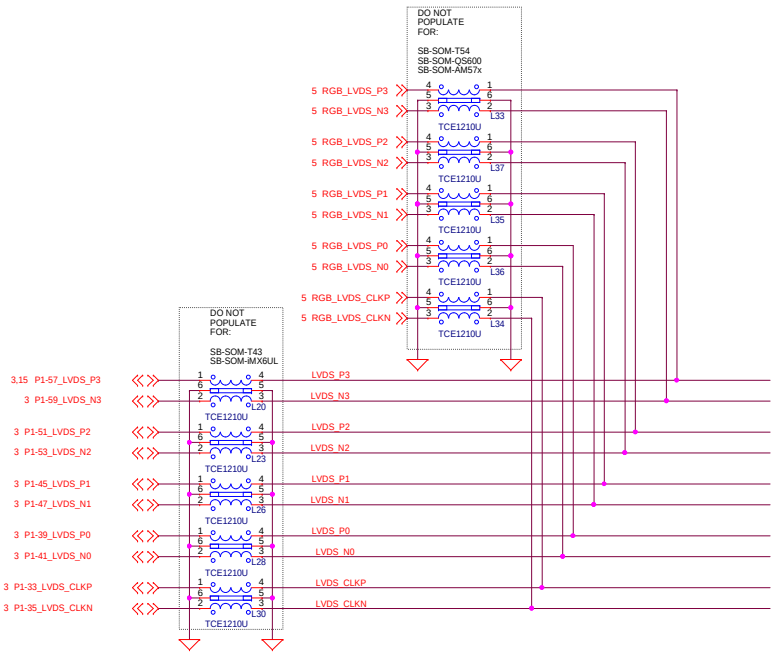
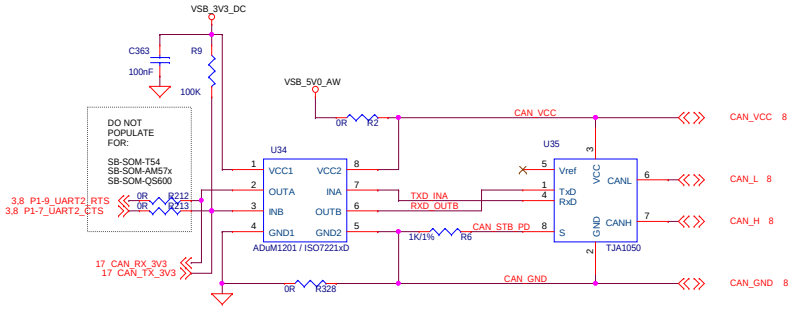
LVDS HEADER



PINOUT SIMILAR TO SB-FX6/SB-T54

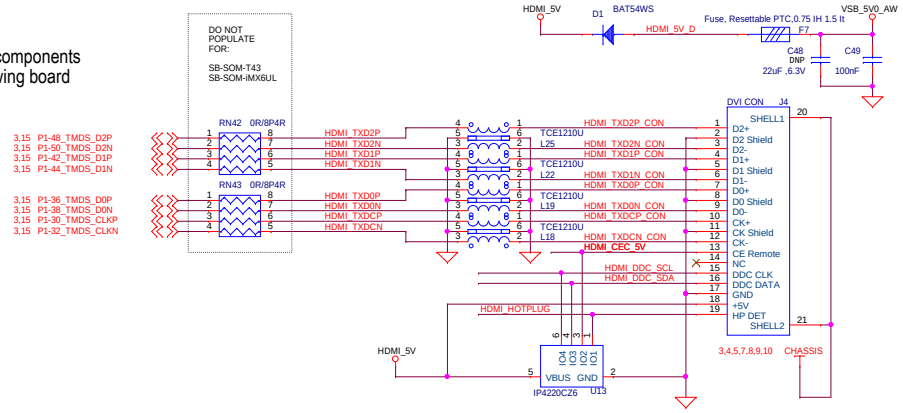


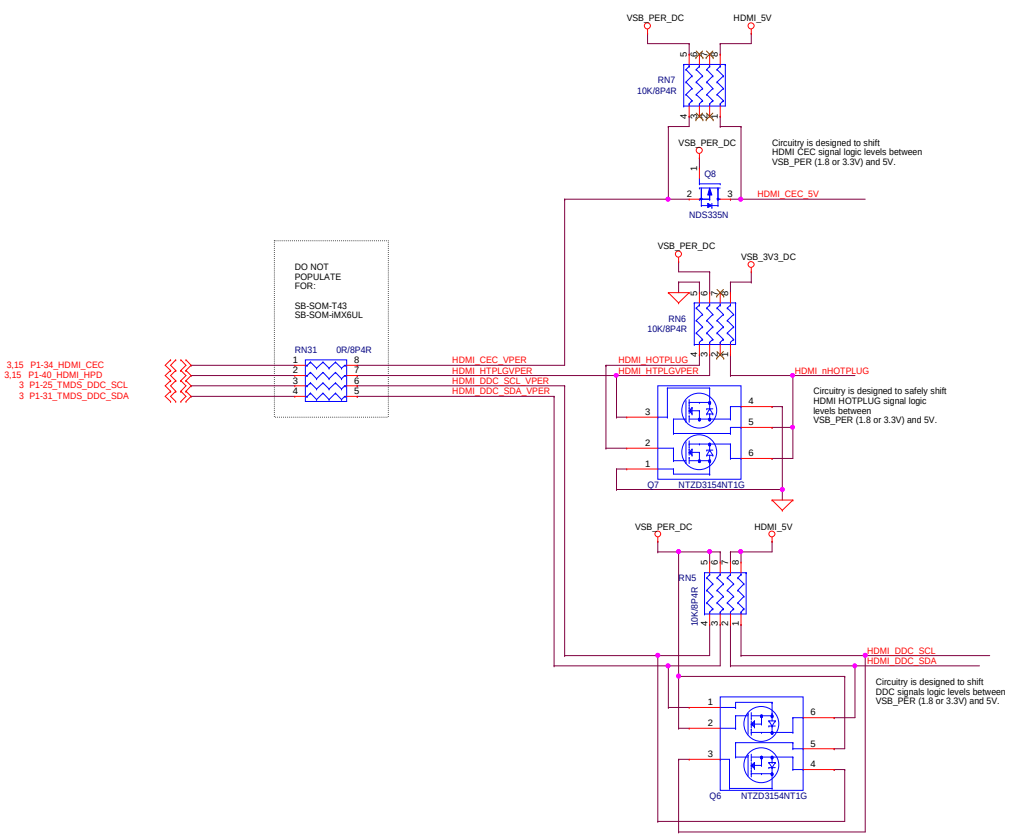
CAN TRANSCEIVER



SoM NATIVE HDMI

NOTE: The native HDMI port components are not populated for the following board configurations:
SB-SOM-iMX6UL*
SB-SOM-T43*





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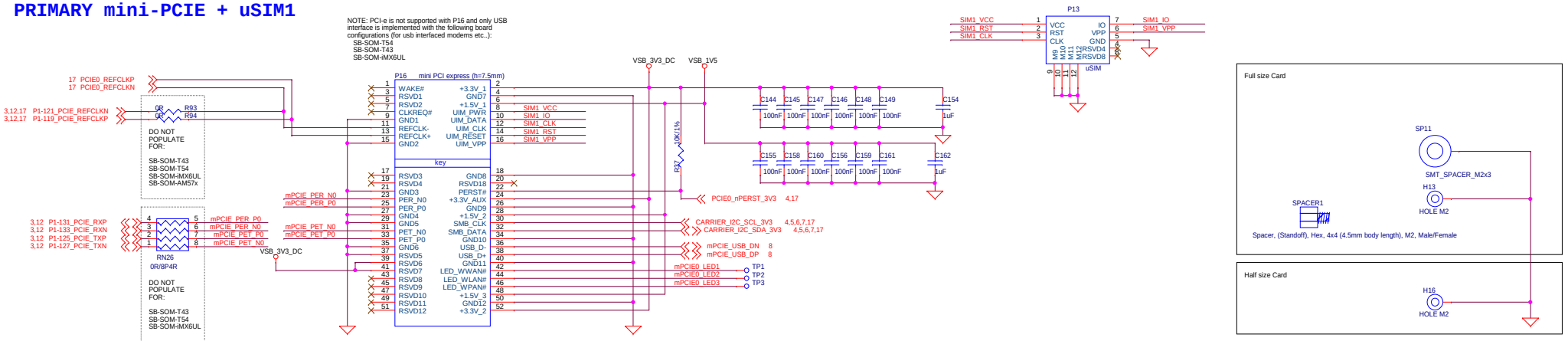
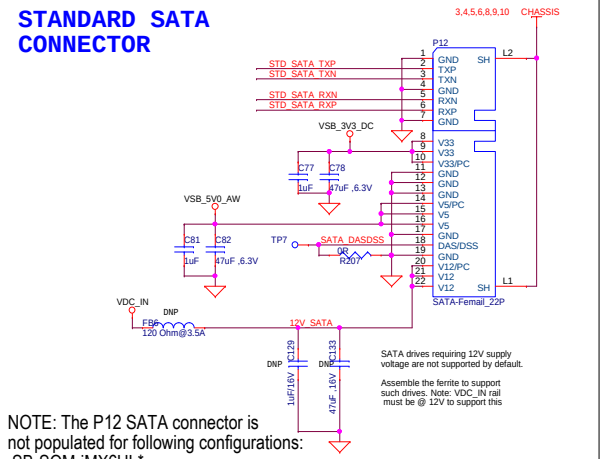
PRIMARY mini-PCIE + uSIM1



STANDARD SATA CONNECTOR



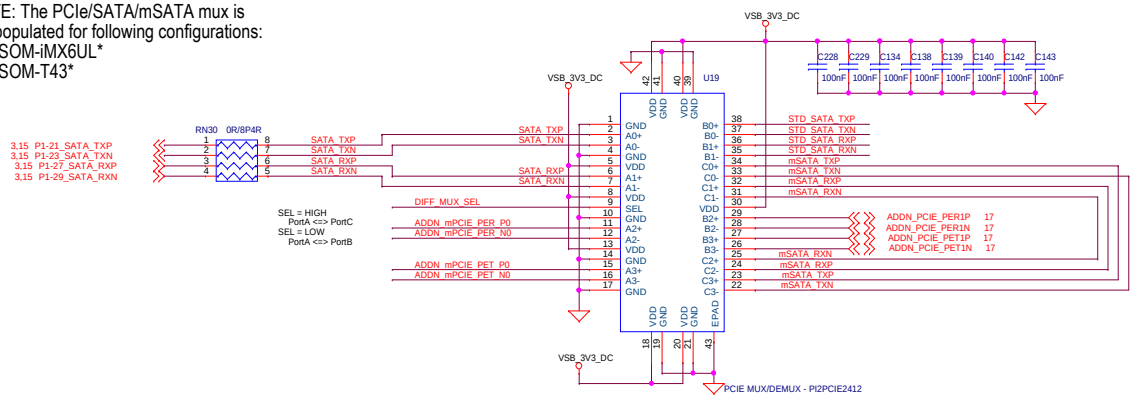
SATA drives requiring 12V supply voltage are not supported by default.

Assemble the ferrite to support such drives. Note: VDC_IN rail must be @ 12V to support this

NOTE: The P12 SATA connector is not populated for following configurations:
SB-SOM-iMX6UL*
SB-SOM-T43*

PCIE/SATA/mSATA MUX

NOTE: The PCIe/SATA/mSATA mux is not populated for following configurations:
SB-SOM-iMX6UL*
SB-SOM-T43*

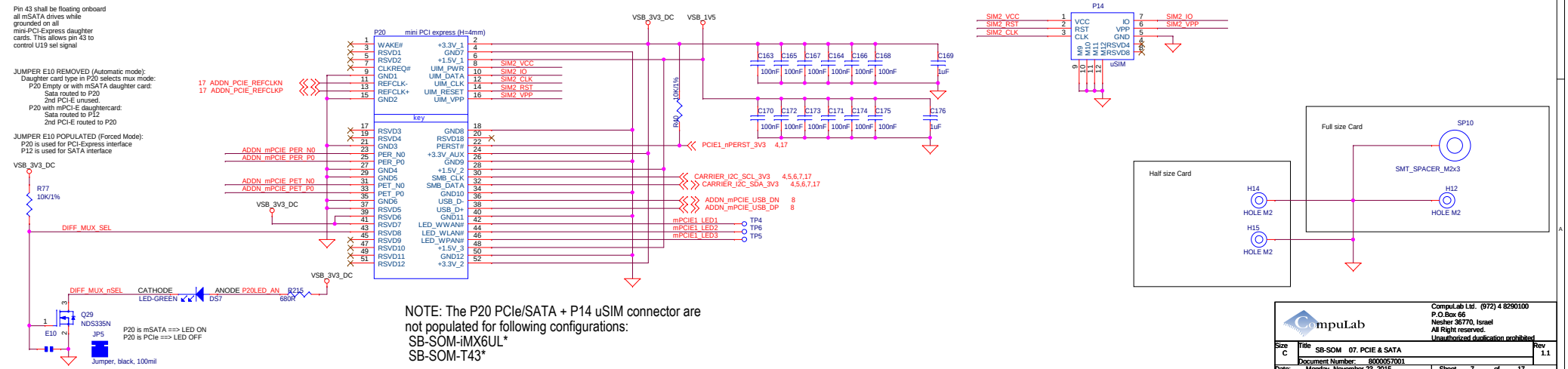


SECONDARY PCIE/mSATA/USB + uSIM2

Pin 43 shall be floating onboard all mSATA drives while grounded on all mini-PCI-Express daughter cards. This allows pin 43 to control U19 sel signal

JUMPER E10 REMOVED (Automatic mode):
Daughter card type in P20 selects mux mode:
P20 Empty or with mSATA daughter card:
Sata routed to P20
2nd PCI-E unused.
P20 with mPCI-E daughtercard:
Sata routed to P12
2nd PCI-E routed to P20

JUMPER E10 POPULATED (Forced Mode):
P20 is used for PCI-Express interface
P12 is used for SATA interface



NOTE: The P20 PCIe/SATA + P14 uSIM connector are not populated for following configurations:
SB-SOM-iMX6UL*
SB-SOM-T43*

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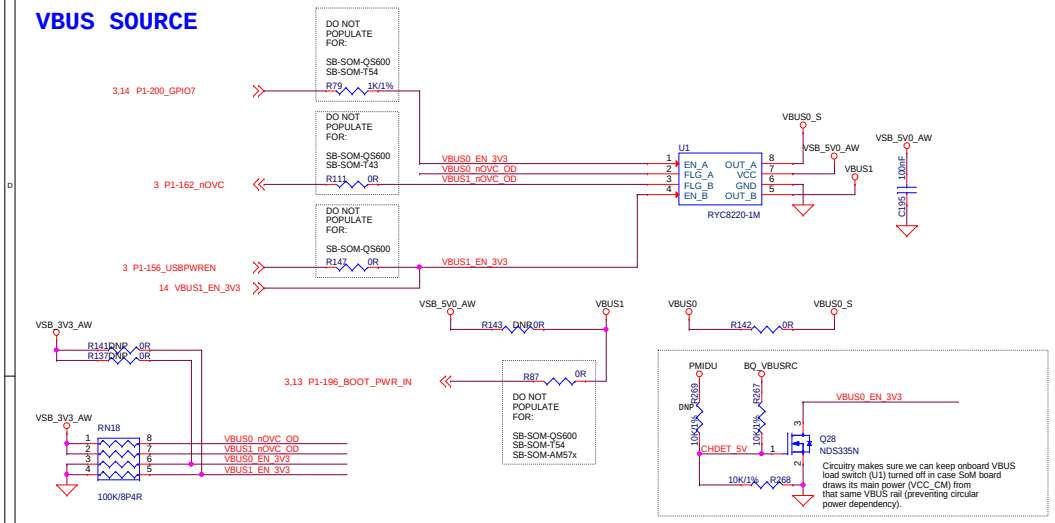
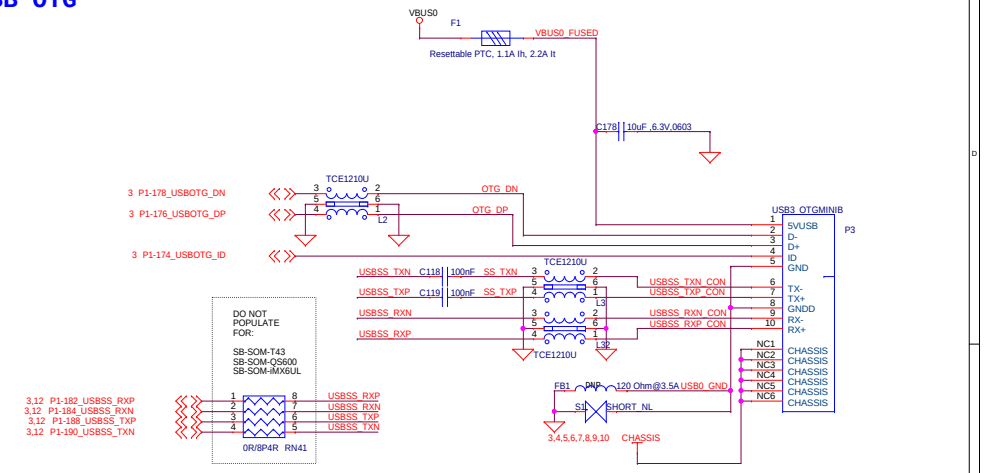
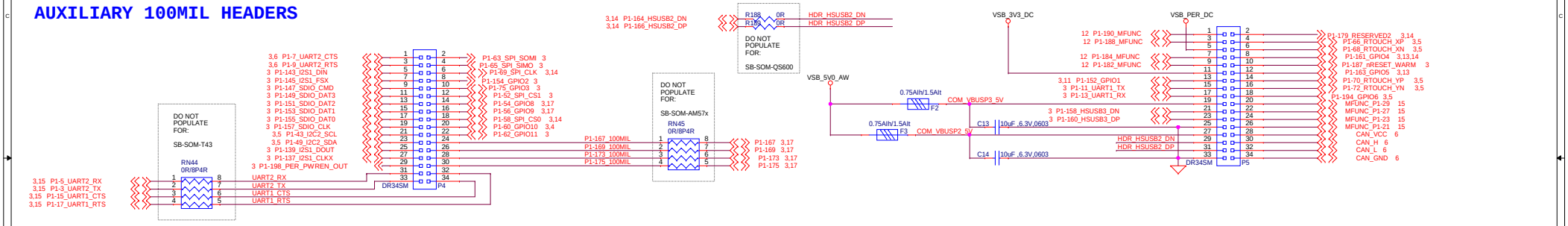
VBUS SOURCE



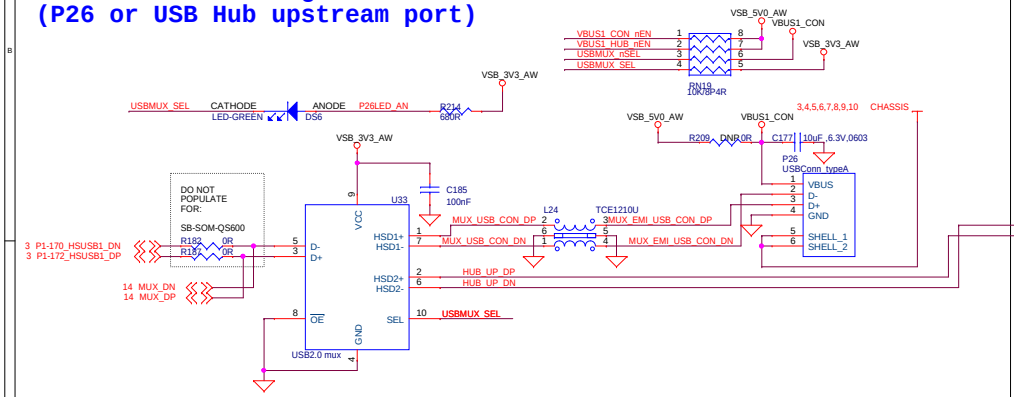
USB OTG



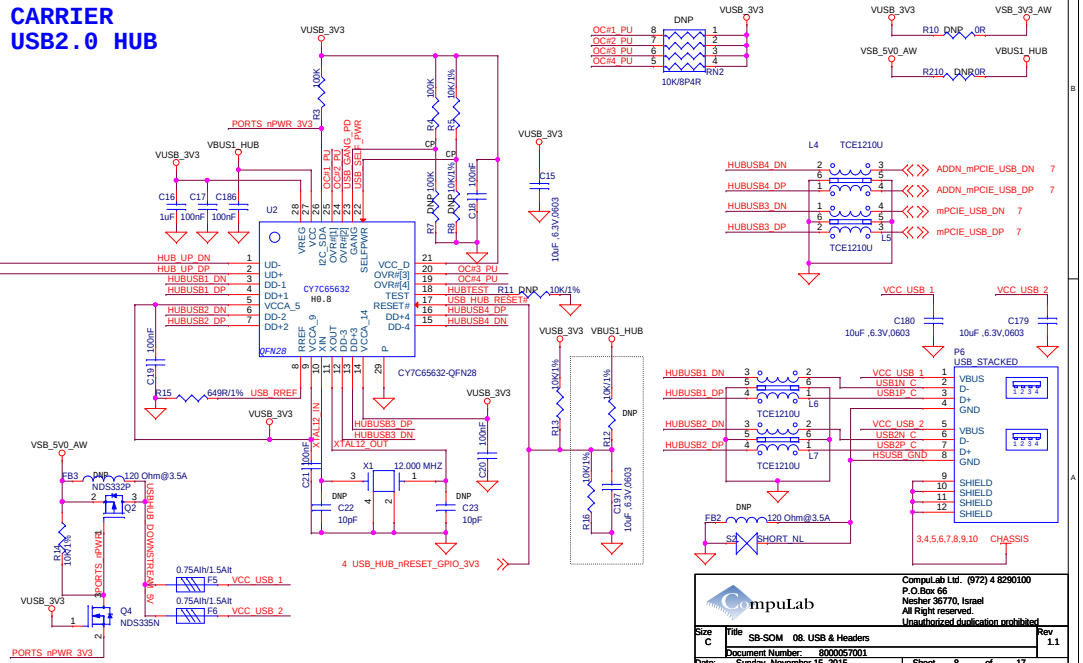
AUXILIARY 100MIL HEADERS



SoM/CoM USB2.0 usage selecor (P26 or USB Hub upstream port)



CARRIER USB2.0 HUB



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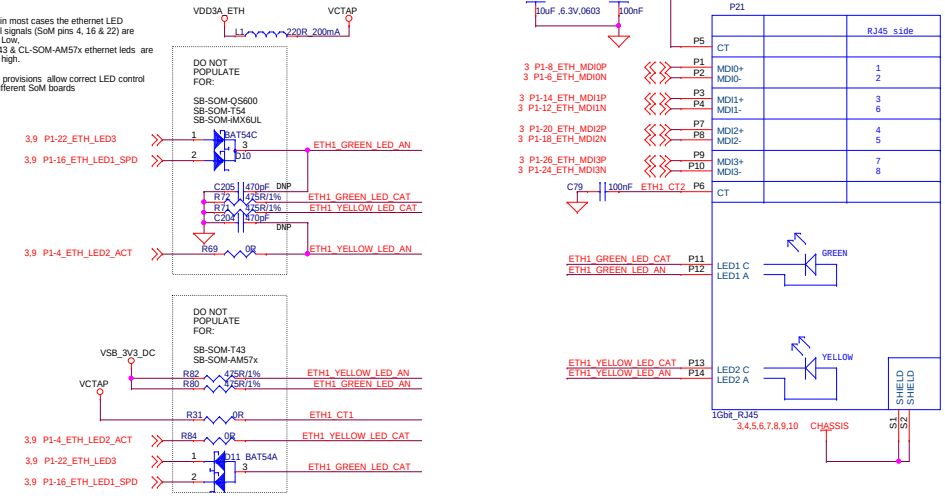
PRIMARY CoM/SoM ETHERNET RJ45

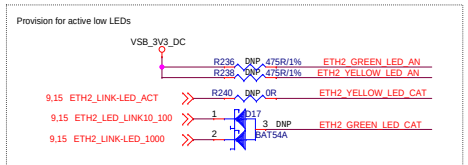
While in most cases the ethernet LED control signals (SoM pins 4, 16 & 22) are active Low,
CM-T43 & CL-SOM-AM57x ethernet leds are active high.

These provisions allow correct LED control with different SoM boards



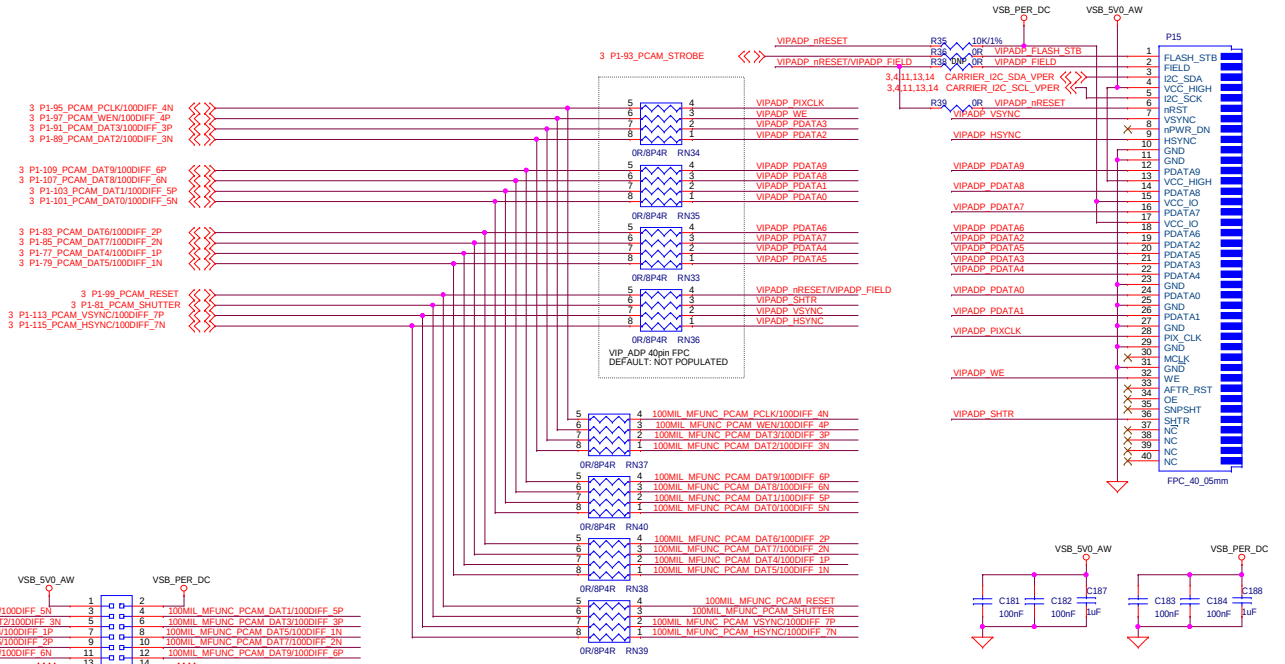
SECONDARY ETHERNET RJ-45

Can be utilized only with following SoM + Carrier Combinations:
1. Stock CM-T43 + SB-SOM-T43 --> LEDs active high



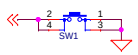
NOTE: The secondary ethernet RJ-45 is not populated for following configurations:
SB-SOM-QS600*
SB-SOM-AM57x*
SB-SOM-iMX6UL*
SB-SOM-T54*

PARALLEL CAMERA INTERFACE OPTIONS

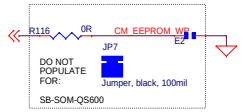


POWER/RESET/BOOT SWITCHES

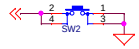
Active low power button input to SoM:
Signal pulled high onboard SoM. SoM behavior may differ with different SoMs. Please refer to SoM specific reference manual for detailed information.

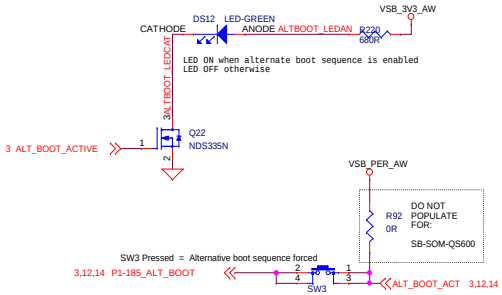


SoM onboard EEPROM write protection feature:
Signal pulled high onboard SoM. SoM behavior may differ with different SoMs. Please refer to SoM specific reference manual for detailed information.



SoM active low reset button input to SoM:
SoM behavior may differ with different SoMs. Please refer to SoM specific reference manual for detailed information.





ALT_BOOT:
T43, T54, AM57x, iMX6UL (pulled LOW on SoM)
LOW - normal boot sequence
HIGH - alternative boot sequence
QS600 (no pull on SOM)
HIGH - normal boot sequence
LOW - alternative boot sequence

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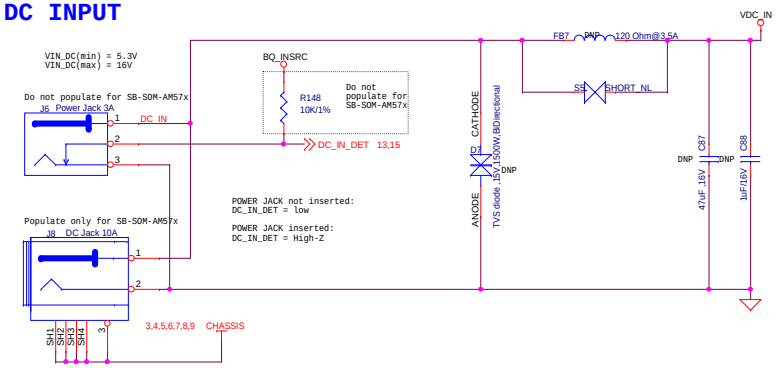
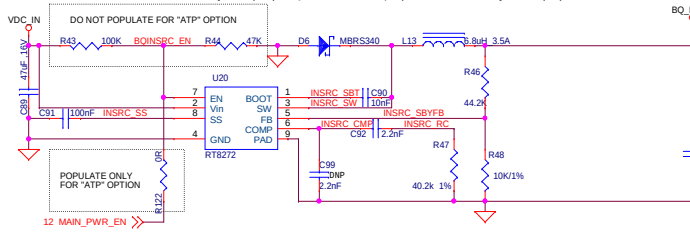
DC INPUT

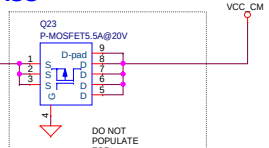


DC-to-5.25V

Vout=Vfb*(1+Rt/Rb)=0.92*(1+44.2/10)=4.9864V.
Note: in case VDC_IN is @ minimum voltage (5.3V),
BQ_INSRC(max) is @ 5.3*0.8 = 4.24V, (still valid for BQ24161 input)

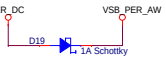


CHARGER BYPASS



VSB_3V3_AW SOURCE (FROM DC)

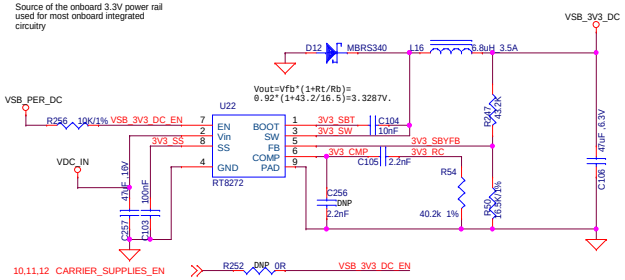
VSB_PER_AW SOURCE (FROM DC)



VSB_5V0_AW SOURCE (FROM DC)

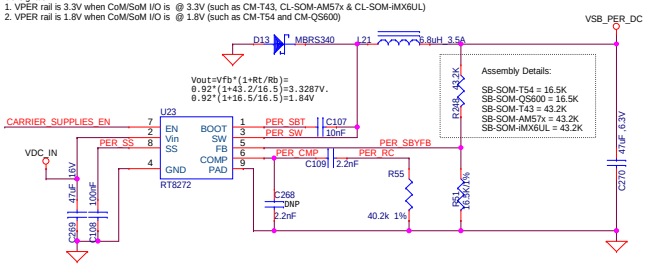
VSB_3V3_DC SOURCE

Source of the onboard 3.3V power rail used for most onboard integrated circuitry

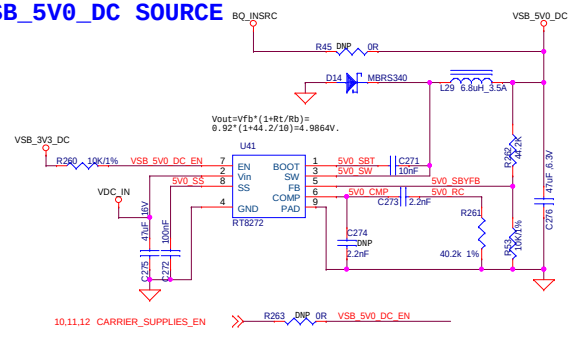


VSB_PER_DC SOURCE

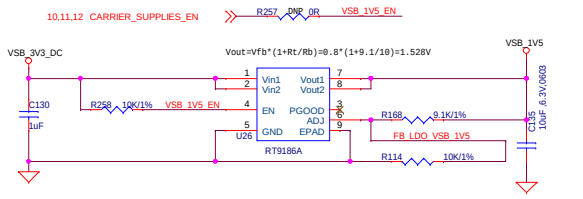
Source of the onboard VPER power rail used for most onboard peripherails interfaced directly with CoM I/O signals.
1. VPER rail is 3.3V when CoM/SoM I/O is @ 3.3V (such as CM-T43, CL-SOM-AM57x & CL-SOM-iMX6UL)
2. VPER rail is 1.8V when CoM/SoM I/O is @ 1.8V (such as CM-T54 and CM-QS600)



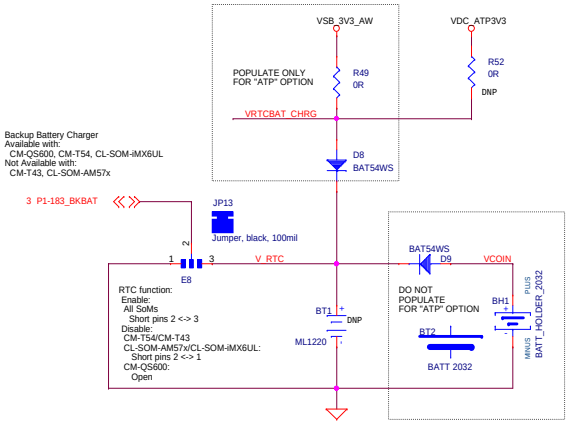
VSB_5V0_DC SOURCE



1V5 SOURCE FOR PCI-e (enabled only when main power source is DC)



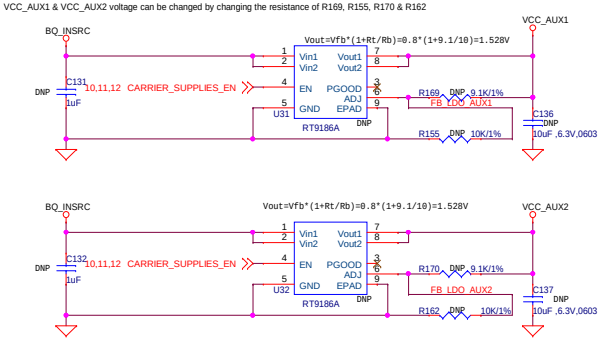
RTC BATTERY



VCC_AUX1 & VCC_AUX2 sources NOT POPULATED BY DEFAULT

These placeholders allow generating additional voltages rails often required by different camera sensors.
The VCC_AUX1 & VCC_AUX2 voltages can be sourced into the sensor from the 100mil camera header

VCC_AUX1 & VCC_AUX2 voltage can be changed by changing the resistance of R169, R155, R170 & R162



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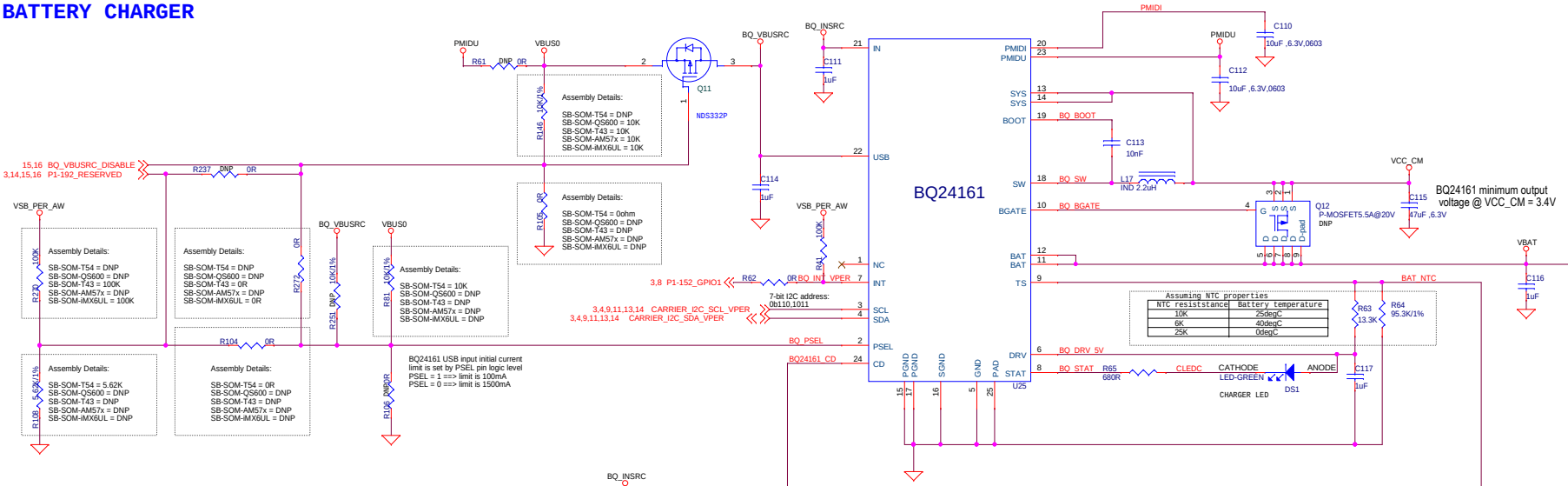
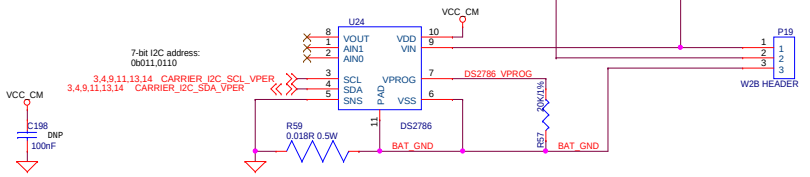
AUTOMATIC POWER SOURCE SWITCHING BETWEEN BATTERY / DC / USB-OTG PORT. & BATTERY CHARGER



NOTE: U21, U24, U25 U38, U39 and their preipherals are not populated with ATP configurations and the following non-ATP configurations:
SB-SOM-QS600
SB-SOM-AM57x

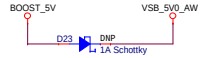
Li-Po Battery Connector & Charging supervisor



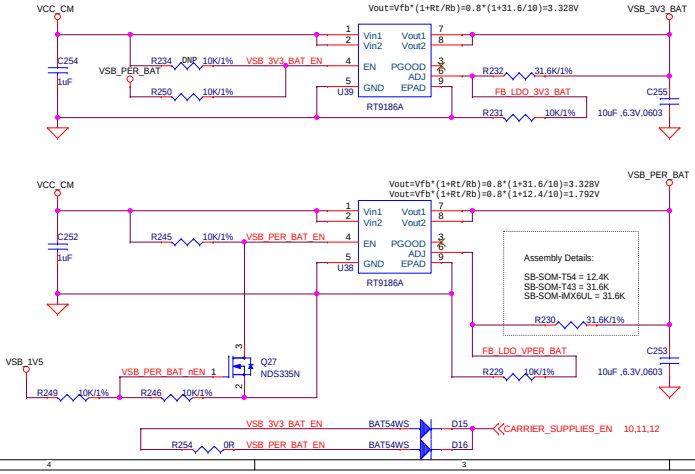
VSB_PER_AW SOURCE (FROM BATTERY/USB)

VSB_3V3_AW SOURCE (FROM BATTERY/USB)

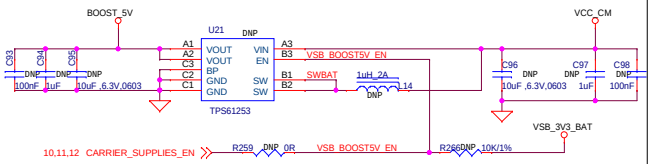
VSB_5V0_AW SOURCE (FROM BATTERY/USB)



VSB_PER_BAT & VSB_3V3_BAT sources



5V SOURCE FROM BATTERY (PROVISION)



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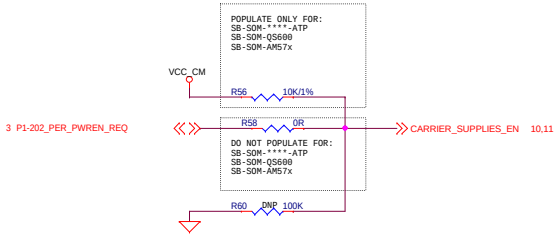
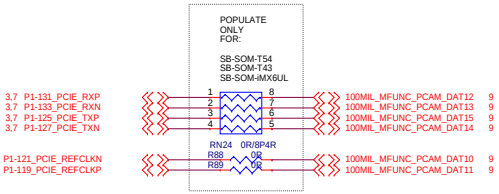
CARRIER SUPPLIES ENABLE LOGIC



T54 (default) drives this high (VCC_CM) as part of powering-up.
T43 (default) pulls this signal up to 3.3V, SW should drive low here when T43 is in low power modes to disable carrier board supplies.
QS600: remove R58, and R56 this should result in VCC_CM voltage"CARRIER_SUPPLIES_EN" pin.
AM57x (default) pulls this high (100k to 3.3V) as part of powering up.
iMX6UL (default) pulls this high (100K to 3.3V) as part of powering up.

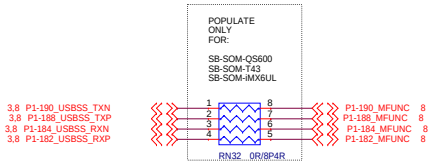
PCI-Express BYPASS

Allows using the PCI-Express lane differential pairs
for alternate functions through a 100MIL header.
Useful with CoM/SoM where PCI-Express function is
not available



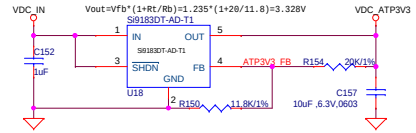
USB3.0 BYPASS

Allows using the USB 3.0 RX & TX differential pairs
for alternate functions through a 100MIL header.
Useful with CoM/SoM where USB3.0 function is
not available

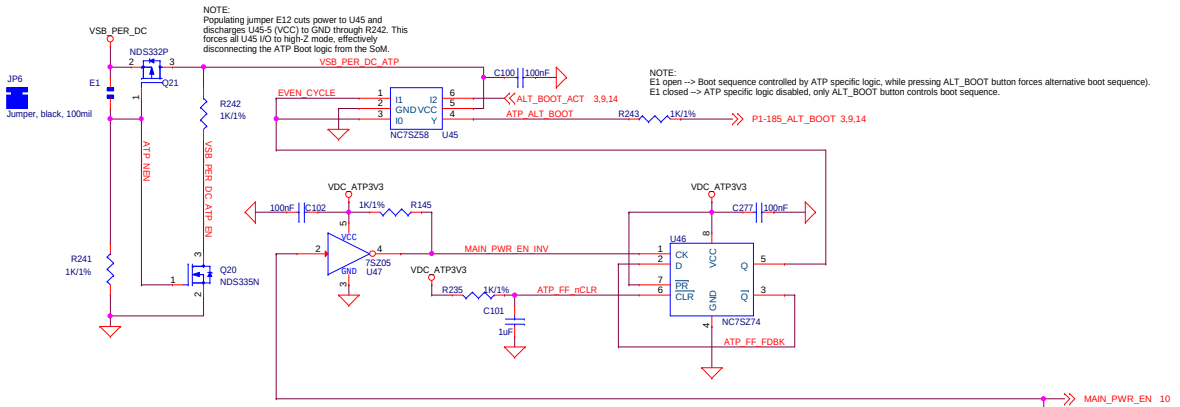


PRODUCTION SPECIFIC PROVISIONS not assembled by default

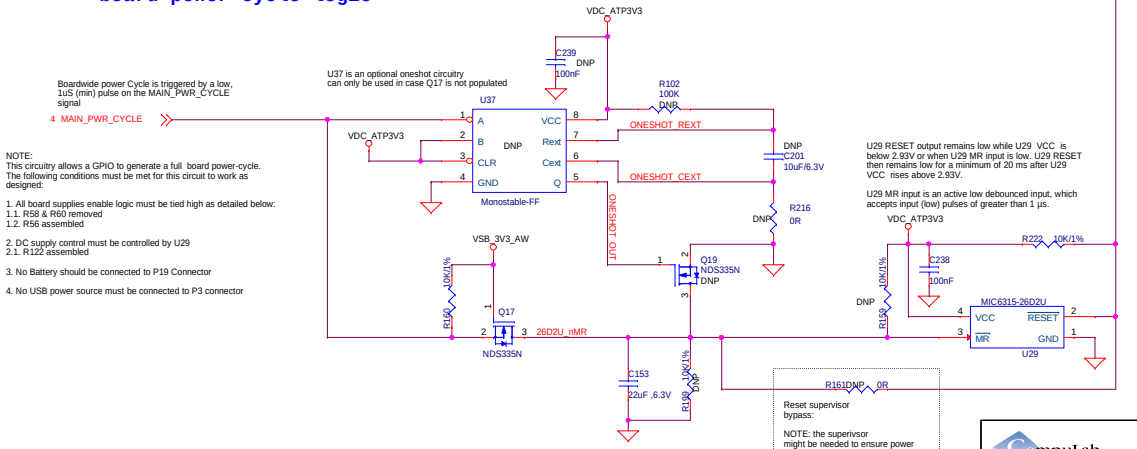
Production power rail - always on



boot sequence auto-toggle logic



board power-cycle logic



NOTE:
This circuitry allows a GPIO to generate a full board power-cycle.
The following conditions must be met for this circuit to work as designed:

1. All board supplies enable logic must be tied high as detailed below:
1.1. R58 & R60 removed
1.2. R56 assembled

2. DC supply control must be controlled by U29
2.1. R122 assembled

3. No Battery should be connected to P19 Connector

4. No USB power source must be connected to P3 connector

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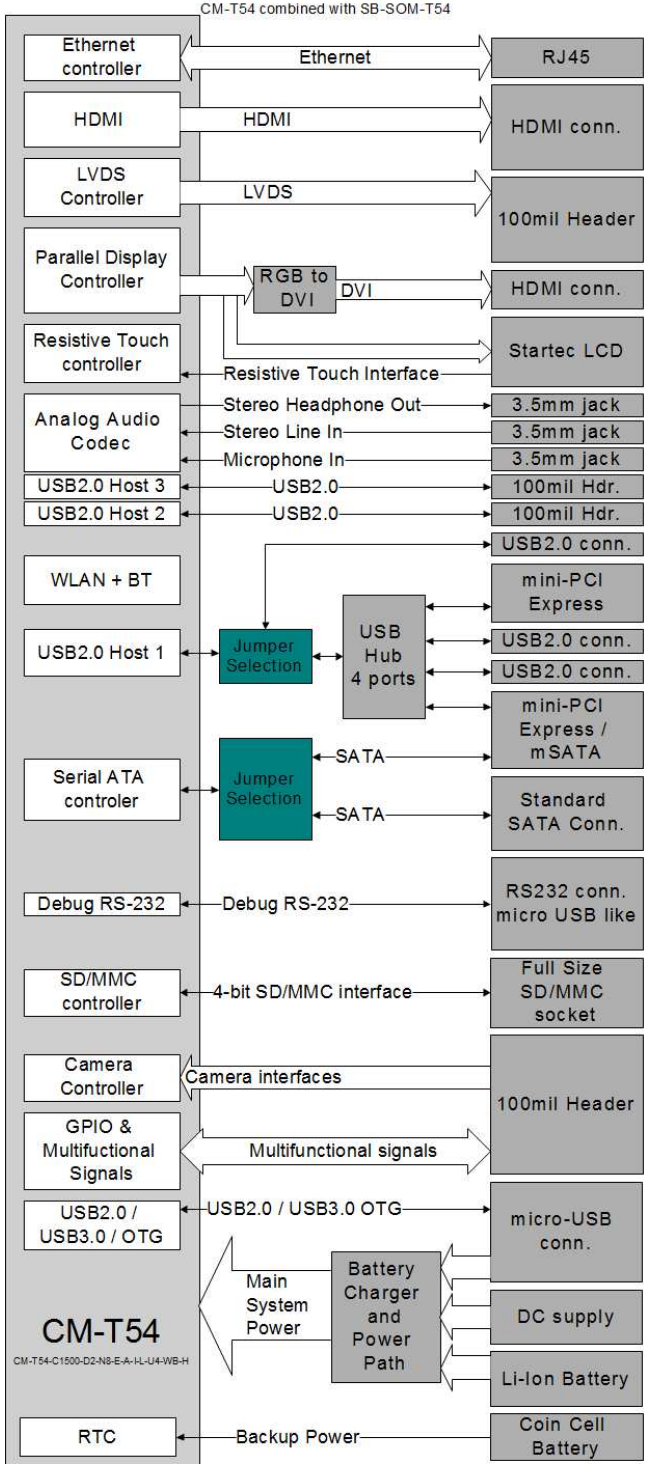
SBC2-T54

CM-T54 combined with SB-SOM-T54



SB-SOM-T54 Specific Provisions Populated only for SB-SOM-T54

SB-SOM-T54 PRIMARY POWER from USB-OTG

Allows CM-T54 to operate from VBUS0 (overcoming the initial 100mA current limit of USB), as described in CM-T54 reference manual chapter 5.5

3,8 P1-196_BOOT_PWR_IN — R103 0R — PMIDU

C196 10uF_6.3V,0603

SB-SOM-T54 PRIMARY I2C BUS

3,8,14 P1-161_GPIO4 — 0R R73 — CARRIER_I2C_SCL_VPER 3,4,9,11,14

3,8 P1-163_GPIO5 — 0R R74 — CARRIER_I2C_SDA_VPER 3,4,9,11,14

SB-SOM-T54 PRIMARY DEBUG UART/RS-232

3,4 P1-111_UARTDBG_TX — R120 0R — RS232_TXD R228 0R — RS232DB_TXD_CON 4

3,4 P1-117_UARTDBG_RX — R119 0R — RS232_RXD R217 0R — RS232DB_RXD_CON 4

SB-SOM-T54 I2C USED FOR DVI DDC

SB-SOM-T54 AC-Adapter detection

P1-181 = VAC_DETECT

VAC_DETECT Default settings:
1. VAC_OK ON request is registered by CM-T54 upon rising of VAC_DETECT voltage above 3.6V(max), or falling of VAC_DETECT voltage below 2.8V(min)
2. In case VCC_CM & BACKUP Battery are not available while VAC_DETECT rises above 3.6V(max), CM-T54 transitions from "NO SUPPLY" power state to "BACKUP" power state.
3. This CM-T54 input is tolerant to voltages between 0V & 10V

3,14,15 P1-181_RESERVED3 — R110 0R — DC_IN_DET 10,15

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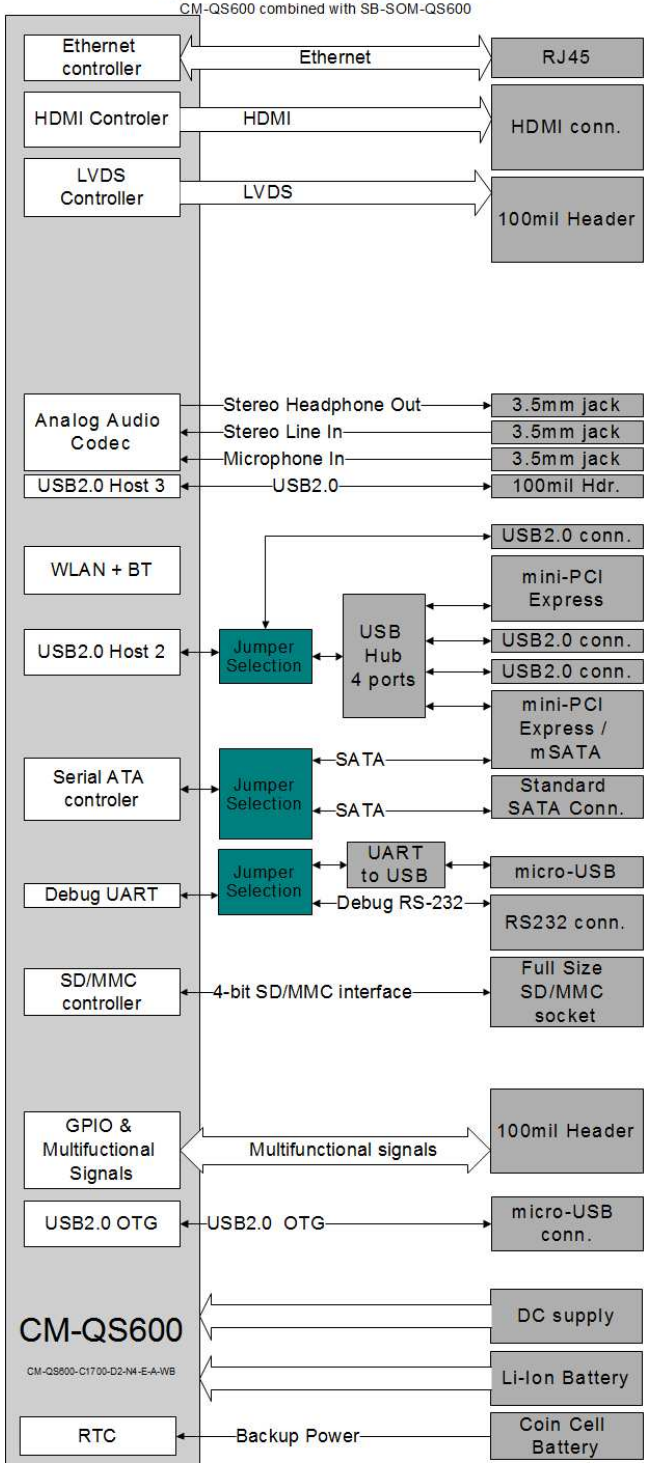
SBC2-QS600

CM-QS600 combined with SB-SOM-QS600



SB-SOM-QS600 Specific Provisions
Populated only for SB-SOM-QS600

SB-SOM-QS600 USB HOST POWER CONTROL

SB-SOM-XXX uses the 3.3V USBPWR_EN function on pin 156 of SoM/CoM interface to enable VBUS (VBUS1 rail) for the USB Hub / P26 USB conenctor (page8). Using pin 156 with SB-SOM-QS600 is not possible since a 3.3V signal is required to enable VBUS1, while a 1.8V GPIO is routed to pin 156 onboard CM-QS600.

To overcome this, we are using pin 200 of CM-QS600 interface, (which has 3.3V GPIO functionality with all CM-QS600 configurations), with SB-SOM-QS600, allowing VBUS1 control by means of 3.3V GPIO.

SB-SOM-QS600 USB Hub upstream port

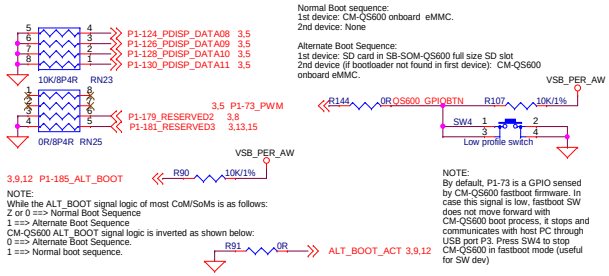
Normally, SB-SOM-XXX uses the SoM USB2.0 port on pins 170 & 172 as the upstream USB port of the carrier USB Hub (page8). CM-QS600 does not implement a USB2.0 interface on pins 170 & 172.

To overcome this, we are using the USB port CM-QS600 implements on pins 164 & 166 as the upstream USB port of SB-SOM-QS600 USB Hub

CM-QS600 BOOT STRAPS & SEQUENCES

Normal Boot sequence:
1st device: CM-QS600 onboard eMMC.
2nd device: None

Alternate Boot Sequence:
1st device: SD card in SB-SOM-QS600 full size SD slot
2nd device (if bootloader not found in first device): CM-QS600 onboard eMMC.



NOTE:
While the ALT_BOOT signal logic of most CoM/SoMs is as follows:
Z or 0 ==> Normal Boot Sequence
1 ==> Alternate Boot Sequence
CM-QS600 ALT_BOOT signal logic is inverted as shown below:
0 ==> Alternate Boot Sequence.
1 ==> Normal boot sequence.

NOTE:
By default, P1-73 is a GPIO sensed by CM-QS600 fastboot firmware. In case this signal is low, fastboot SW does not move forward with CM-QS600 boot process, it stops and communicates with host PC through USB port P3. Press SW4 to stop CM-QS600 in fastboot mode (useful for SW dev)

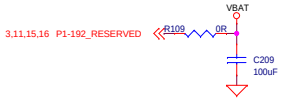
Power-Down Parallel RGB Shifters

Keep Parallel RGB interface disabled with SB-SOM-QS600 since this interface is not available with CM-QS600 SoM/CoM

SB-SOM-QS600 PRIMARY I2C BUS

SB-SOM-QS600 POWER

This enables operation of CM-QS600 from battery
Please note that while CM-QS600 power can be supplied directly from battery, most carrier board components require DC power source to be available for normal operation



SB-SOM-QS600 GPIO Expander Interrupt

SB-SOM-XXX uses the GPIO function on pin 60 of SoM/CoM interface as an interrupt for SB-SOM-XXX onboard gpio-expander. Using pin 60 with CM-QS600 is not possible since no GPIO is available on CM-QS600 pin 60 under certain conditions (with WB option of SoM).
To overcome this we are using pin 161 of SoM/CoM interface, (which has GPIO functionality with all CM-QS600 configurations), with SB-SOM-QS600

SB-SOM-QS600 Ethernet LEDs

NOTE: QS600 ethernet controller must be properly configured for ethernet LEDs to operate correctly since default config does not comply with SODIMM204 pinout

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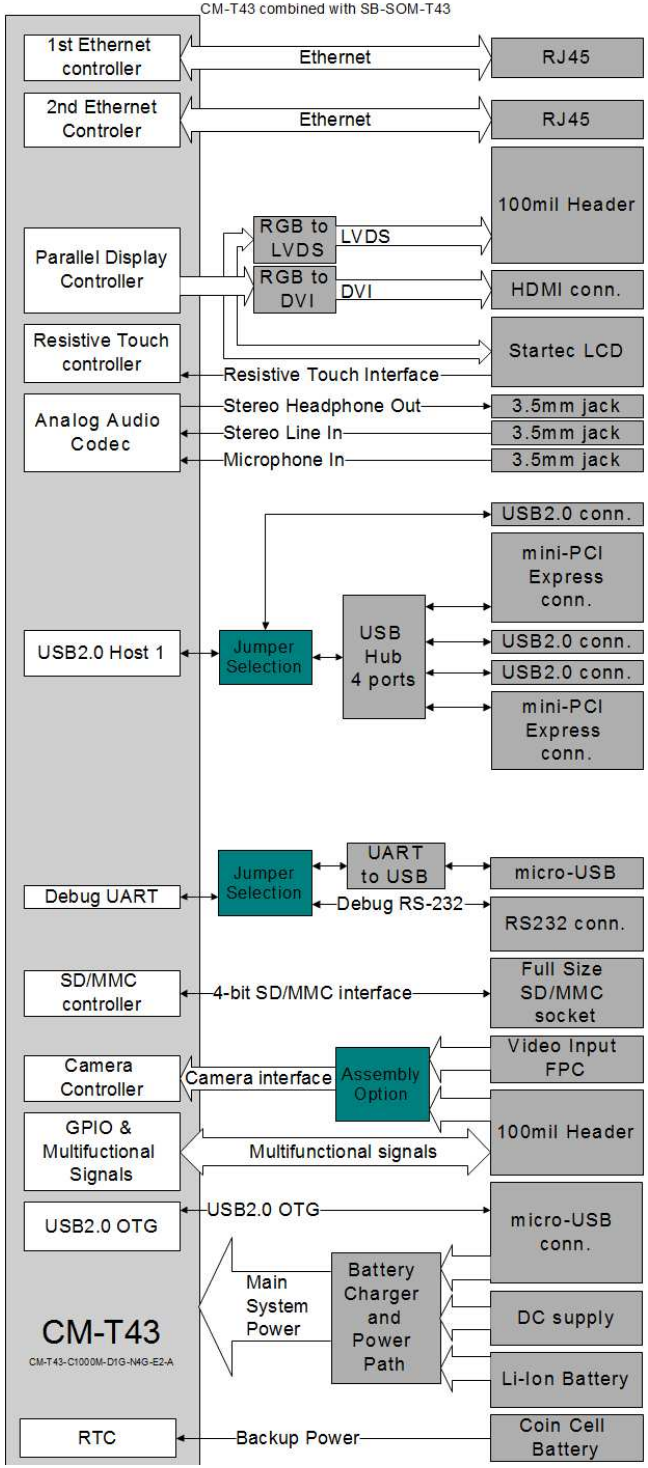
SBC-T43

CM-T43 combined with SB-SOM-T43



SB-SOM-T43 Specific Provisions
Populated only for SB-SOM-T43

Alternate usage of SATA signals

CM-T43 does not implement the SATA interface.
This provision allows SB-SOM-T43 to route signals otherwise used for SATA, to a 100mil header

SB-SOM-T43 CAN BUS

SB-SOM-T43 PRIMARY DEBUG UART/RS-232

SB-SOM-T43 I2C USED FOR DVI DDC

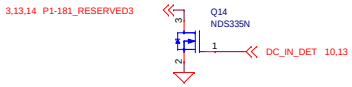
USB1 Host VBUS monitoring

CM-T43 does not implement the BOOT_PWR_IN function on carrier board interface pin 196.
This provision allows CM-T43 to monitor VBUS1 with SB-SOM-T43 board.

SB-SOM-T43 AC POWER & Detection

```
CM-T43 pin 181 = AC_DET

AC_DET Default settings:
1. Pulled to VCC_CM onboard CM-T43
2. Falling edge on AC_DET triggers
transition of CM-T43 from OFF/SUSPED
to WAIT_PWR_EN state.
Normally, CM-T43 then transitions from
WAIT_PWR_EN to ACTIVE state within
20seconds.
```



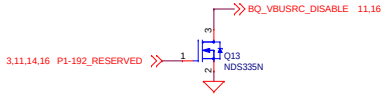
VBUS0 (OTG port) load switch control

CM-T43 can control VBUS0 source (U1 load switch) onboard SB-SOM-T43 through signal on P1-200.
Refer to CM-T43 hardware reference manual for additional details

USB CHARGER LOGIC

CM-T43 drives P1-192_RESERVED
HIGH (3.3V) whenever a USB charger is
detected on the device/host USB port
(P3 USB OTG connector, CM-T43 pins 176 & 178).
Please refer to CM-T43 hardware reference manual for additional details

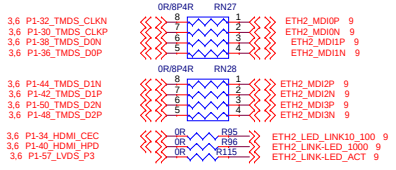
This circuitry makes sure of that if CM-T43 detects a USB charger connected to P3 connector (USB OTG), SB-SOM-T43 can generate VCC_CM (main power rail for CM-T43) from VBUS0 (assuming this rail is the input from the detected charger), allowing the system to be powered from USB power source. Otherwise, assuming VBUS0 is generated onboard SB-SOM-T43, VCC_CM cannot be generated from VBUS0 (preventing reverce power dependency, since in that case VBUS is actually generated from VCC_CM).



CM-T43 2nd ETHERNET (Alternate usage of HDMI signals)

CM-T43 does not implement the HDMI interface.
CM-T43 implements a 2nd ethernet interface, using the signals normally used for HDMI.

This provision allows SB-SOM-T43 to route signals otherwise used for HDMI, to the secondary RJ-45 connector allowing SB-SOM-T43 to make use of the 2nd ethernet port available with CM-T43



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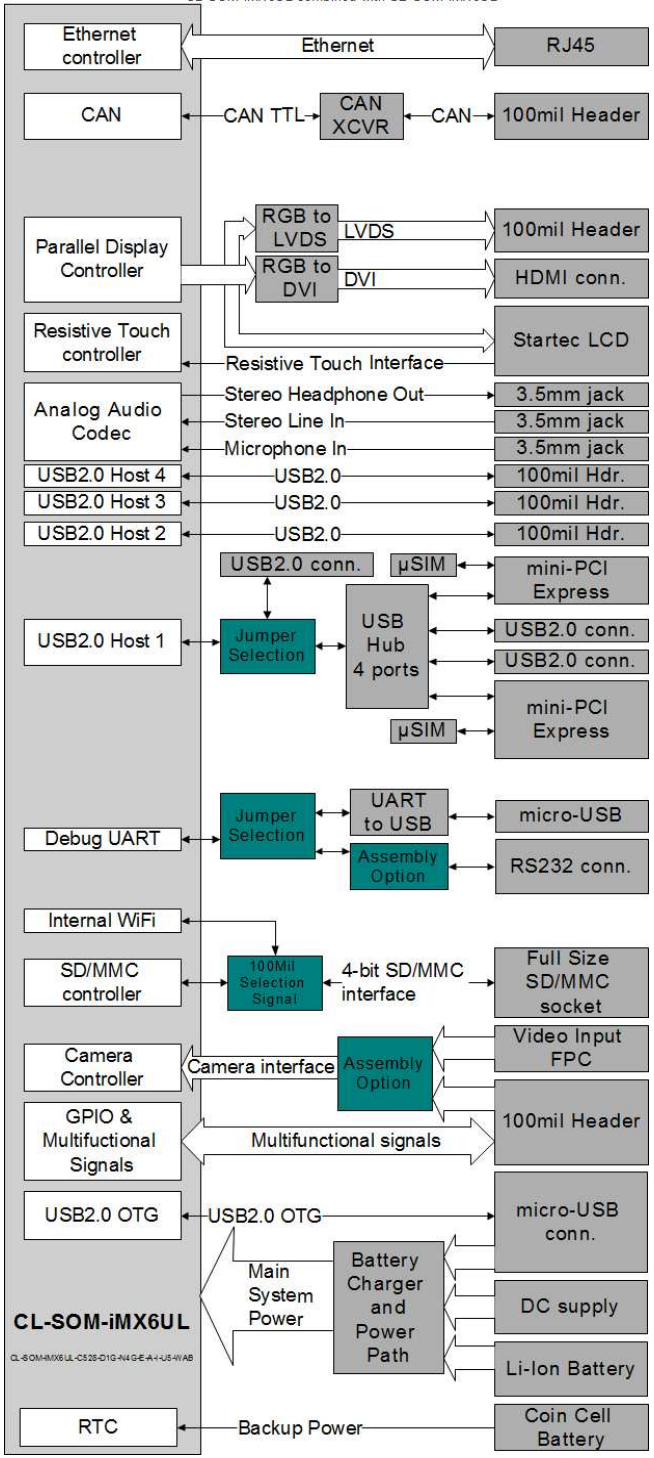
SBC-iMX6UL

CL-SOM-iMX6UL combined with SB-SOM-iMX6UL



SB-SOM-iMX6UL Specific Provisions
Populated only for SB-SOM-iMX6UL

USB CHARGER LOGIC

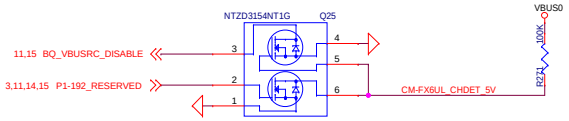
CL-SOM-iMX6UL drives the P1-192_RESERVED open drain signal LOW whenever a USB charger is detected on the device/host USB port (P3 USB OTG connector,CL-SOM-iMX6UL pins 176 & 178). P1-192 is only 3.3V tolerant.
Please refer to CL-SOM-iMX6UL hardware reference manual for additional details.

This circuitry makes sure that if CL-SOM-iMX6UL detects a USB charger connected to P3 connector (USB OTG), SB-SOM-iMX6UL will be able to source VCC_CM (main power rail for CL-SOM-iMX6UL) from VBUS0 (assuming this rail is the input from the detected charger), allowing the system to draw its main power from a USB charger on P3 OTG port (start from USB charger, etc..). Otherwise, assuming VBUS0 is generated onboard SB-SOM-iMX6UL, VCC_CM cannot be generated from VBUS0 (preventing reverse power dependency, since in that case VBUS0 is actually generated from VCC_CM).

No DC Power & Dead Battery (only power source is USB) case:

Since BQ24161 USB power input is open by default (allowing BQ24161 to source VCC_CM from VBUS0). system will be able to start from USB charger on P3.
The drawback here, is that when a VBUS0 is generated from a simple upstream USB host port (not a charger), the system would constantly try to start, until a chrager is connected to P3 with the following infinite loop:

1. Start
2. Detect that upsteram USB is not a charger
3. Power-off
4. repeat from step 1 above



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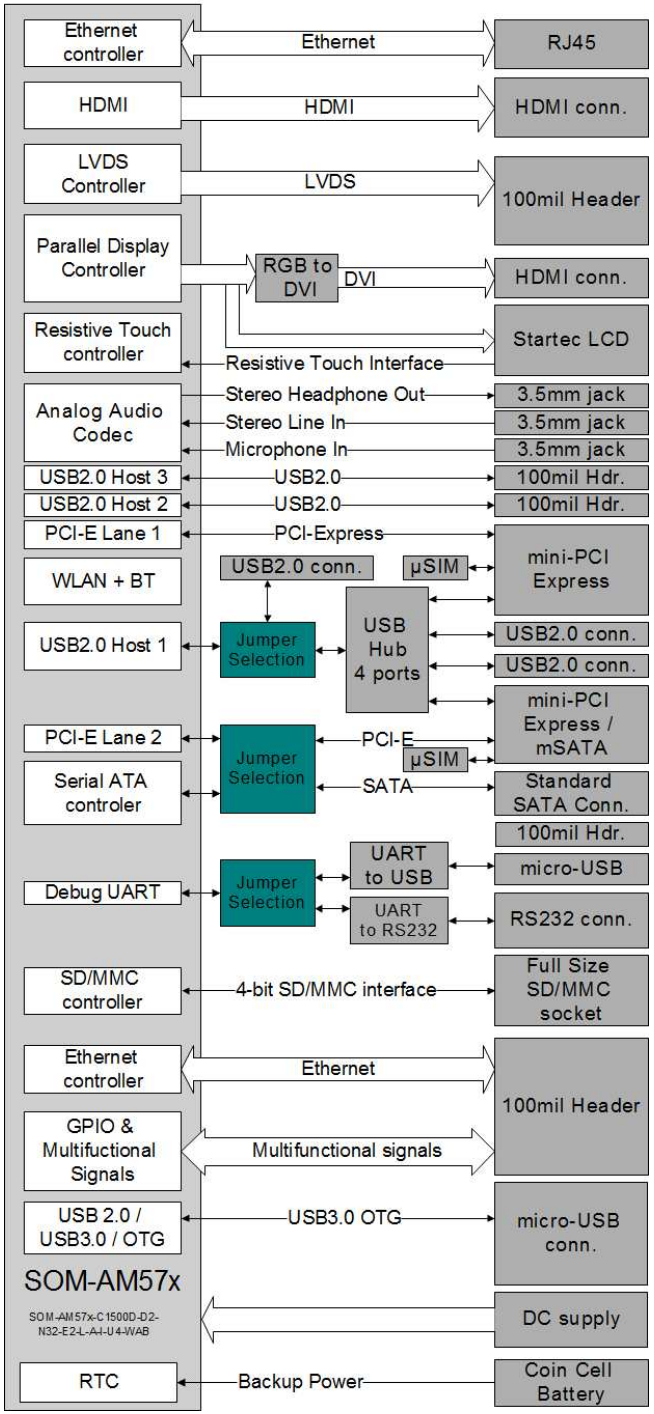
SBC-AM57X

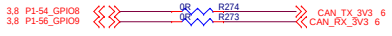
CL-SOM-AM57X combined with SB-SOM-AM57x



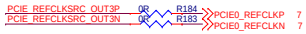
SB-SOM-AM57x Specific Provisions
Populated only for SB-SOM-AM57x

CAN bus

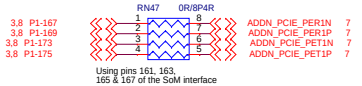
SOM-AM57x DCAN1 interface is exposed through CL-SODIMM pins 54 & 56.



Provision to source PCIE0 REFCLK from GENERATOR to mini-PCI-E connector

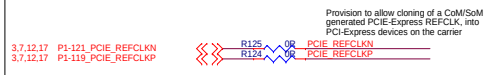


2nd PCI-Express Provision

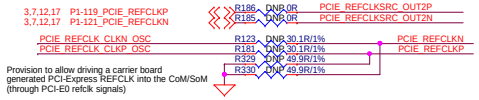


Using pins 161, 163, 165 & 167 of the SoM interface as PCI-Express RX & TX

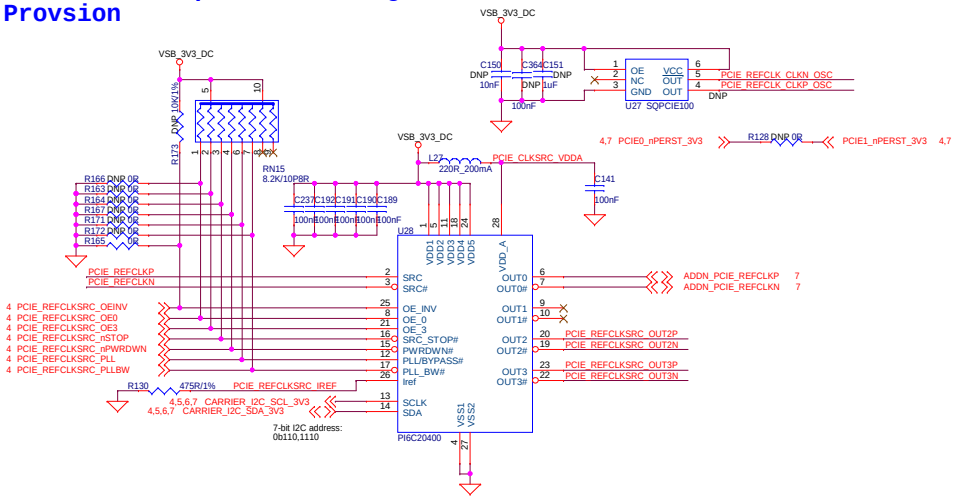
Provision to drive REFCLK GENERATOR from CoM/SoM sourced PCIE0 REFCLK



Provision to source generator source REFCLK from onboard source (U27)



SB-SOM PCI-Express REFCLK generator Provsion



Size	Title	Rev
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