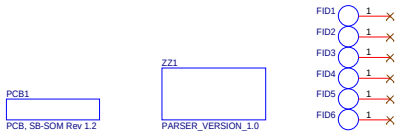
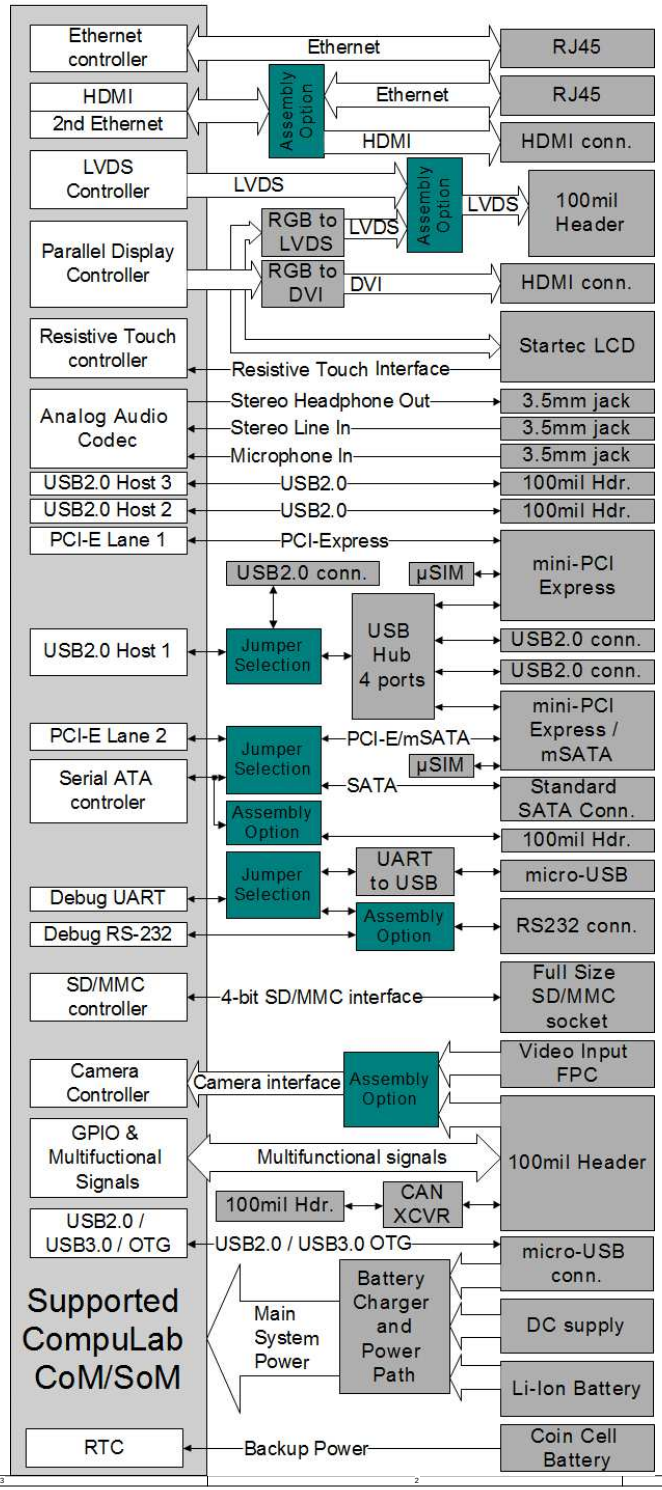
SB-SOM

BOARD REVISION: 1.2


```
CARRIER BOARD PRIMARY I2C BUS SLAVES (7bit address):
-----------------------------------------------------------------------
0b010,0000 - Carrier GPIO Expander
0b011,0110 - DS2786 Battery Supervisor
0b011,1001 - DVI Transmitter
0b101,0100..0b1010111 - Carrier ID EEPROM (except SB-SOM-T43)
0b101,0000..0b1010011 - Carrier ID EEPROM (SB-SOM-T43 only)
0b110,1011 - BQ24161 battery charger & power-path
0b110,1110 - PCI-E REFCLK fanout
```



SB-SOM rev1v2



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BOARD REVISION: 1.0

1. Initial Revision with support for the following SoMs:
1.1. CM-T43
1.2. CM-T54
1.3. CM-QS600

BOARD REVISION: 1.1

1. Power supply scheme changed to improve battery/usb powered system operation.
2. Added initial support for CL-SOM-iMX6UL board.
3. Added initial support for CL-SOM-AM57x board.
4. Board phyiscal dimensions increased to improve usability
5. Improved (silk) description of various board jumpers, buttons, LEDs and connectors.
6. Added production provisions
7. Added GPIO button to be used with CM-QS600
8. Improved backlight driver circuitry
9. Added pads for solderable spacers to comply with new SOM mechanical requirements
10. Removed obsolete PCIe spacers, replaced some with simple mechanical holes

BOARD REVISION: 1.2

1. Added initial support for CL-SOM-iMX7 board.
2. Changed CAN transceiver input to 100mil header. Enabling easy evaluation of each CAN bus available with SOM under evaluation, no matter which SOM I/O pin has CAN bus functionality.
3. Fixed BUG in backlight circuitly.
4. Added active driver to CARREIR_SUPPLIES_EN signal
5. Added a jumper for ALT_BOOT (force ALT_BOOT)
6. Added a jumper for 120Ohm CAN bus termination enable/disable

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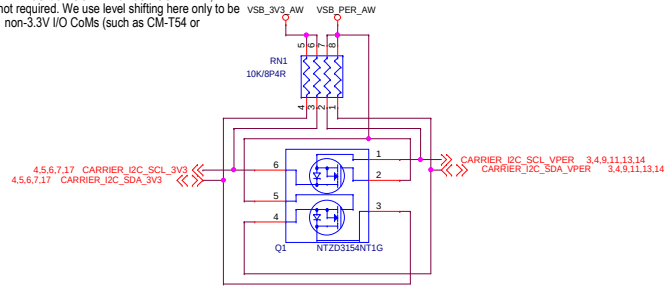
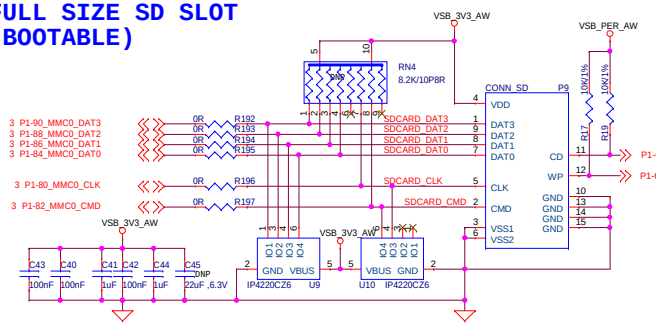
CARRIER BOARD PRIMARY I2C BUS LEVEL SHIFT

Circuitry is designed to shift
I2C signals logic levels between
VSB_PER (1.8 or 3.3V) and 3.3V.

NOTE: In case CoM/SoM I/O is @ 3.3V levels, such as CM-T43/CL-SOM-iMX6UL/CL-SOM-AM57x/CL-SOM-iMX7, level shifting is not required. We use level shifting here only to be compatible with non-3.3V I/O CoMs (such as CM-T54 or CM-QS600)

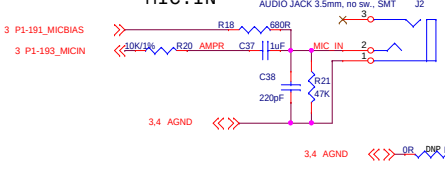


FULL SIZE SD SLOT (BOOTABLE)

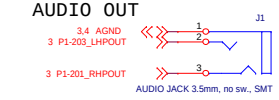


ANALOG AUDIO

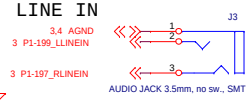
MIC.IN



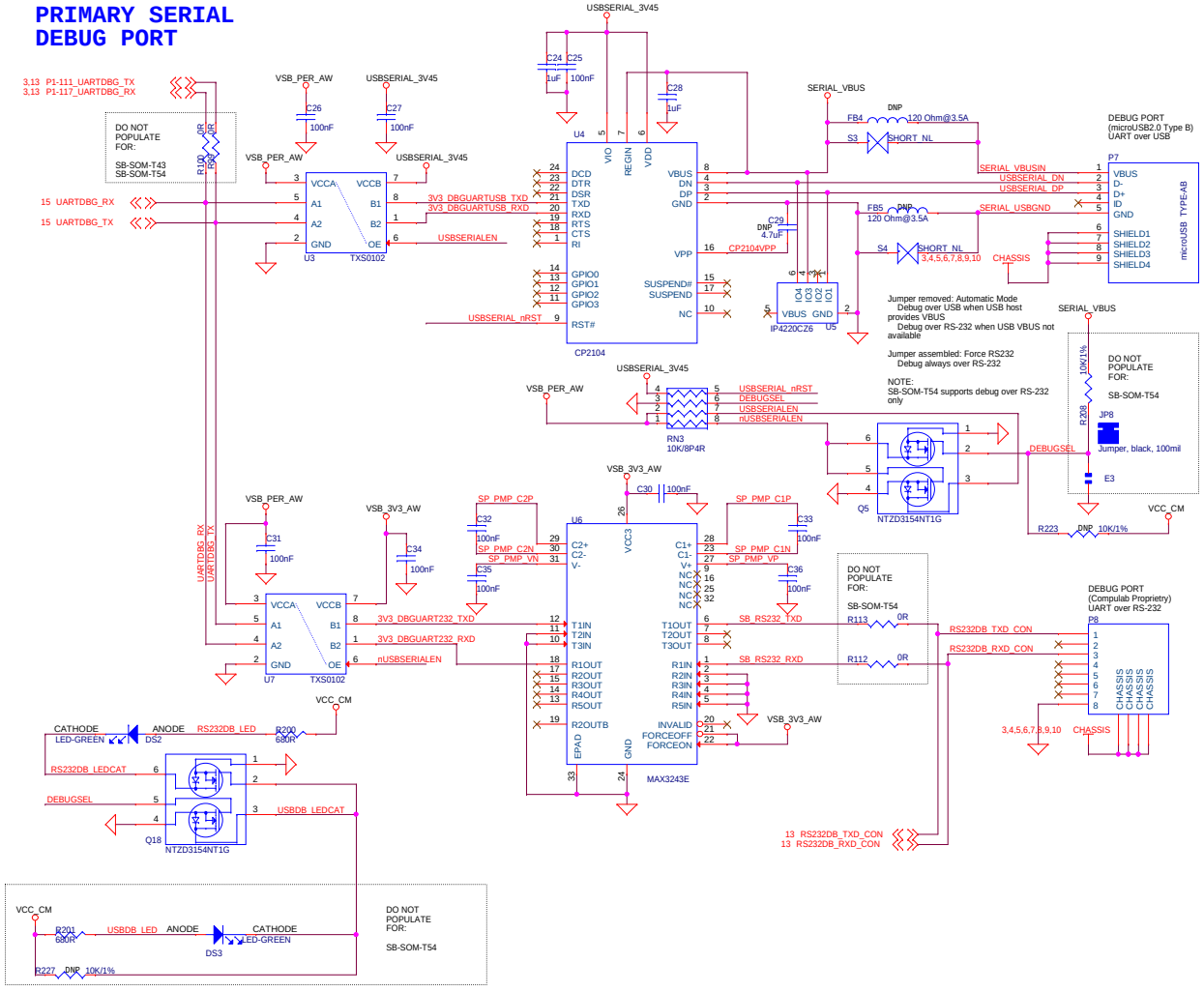
AUDIO OUT



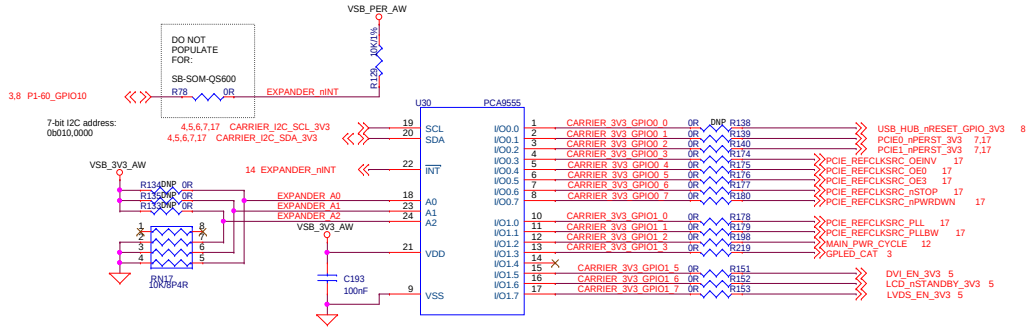
LINE IN



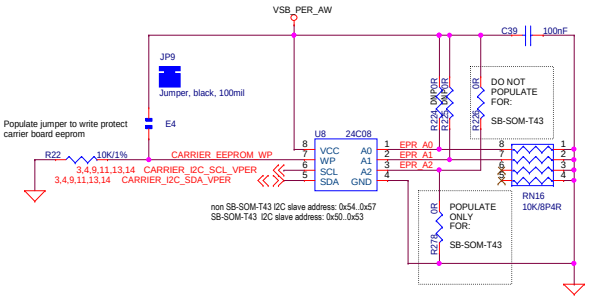
PRIMARY SERIAL DEBUG PORT



CARRIER GPIO EXPANDER



CARRIER BOARD EEPROM



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SoM Screws

3.5mm screws for:
SB-SOM-AM57x
SB-SOM-iMX7

SCREW1
SCREW, M2, 3.5mm, PAN HEAD

SCREW2
SCREW, M2, 3.5mm, PAN HEAD

SoM spacers

73mm SoM
SP16 SP15 SMT_SPACER_M2x3 SMT_SPACER_M2x3

60mm SoM
SP18 SP17 SMT_SPACER_M2x3 SMT_SPACER_M2x3

42mm SoM
SP22 SP21 SMT_SPACER_M2x3 SMT_SPACER_M2x3

36mm SoM
SP20 SP19 SMT_SPACER_M2x3 SMT_SPACER_M2x3

ALTERNATE BOOT SEQUENCE ENABLED LED

VSB_PER_AW
LED is on when alternate boot sequence is enabled
C200 100nF
U40 NC7SZ57
3,9,12,14 P1-185_ALT_BOOT
ALT_BOOT_ACT 9,12,14
ALT_BOOT_ACTIVE 9

U40 output = (NOT INPUT0) * (NOT INPUT2) + INPUT2 * INPUT 1 = P1-185_ALT_BOOT xor ALT_BOOT_ACT

Basic Carrier Board Peripherals Power LED

VSB_3V3_AW
R202 680R
3P3 LED
DS4 LED-GREEN
ANODE
CATHODE

SoM/CoM Primary Power LED

VCC_CM
R203 680R
CM LED
DS5 LED-GREEN
ANODE
CATHODE

Carrier Board GPIO Controlled LED

VSB_3V3_AW
R218 680R
4 GPLED_CAT
DS10 LED-GREEN
CATHODE
ANODE
GP LED

CoM/SoM Mechanic Holes

H1 HOLE M2
H2 HOLE M2
H3 HOLE M2
H4 HOLE M2
H5 HOLE M2
H6 HOLE M2

Carrier Board Mechanic Holes

3,4,5,6,7,8,9,10 CHASSIS
H7 H8 H9 H10

P1 SODIMM-204-BOARD

TOP

1	GND1		
3	UART2_TX	8,15 P1-3_UART2_TX	
5	UART2_RX	8,15 P1-5_UART2_RX	
7	UART2_CTS	6,8 P1-7_UART2_CTS	
9	UART2_RTS	6,8 P1-9_UART2_RTS	
11	UART1_TX	8 P1-11_UART1_TX	
13	UART1_RX	8 P1-13_UART1_RX	
15	UART1_CTS	8,15 P1-15_UART1_CTS	
17	UART1_RTS	8,15 P1-17_UART1_RTS	
19	GND2		
21	SATA_TX+	7,15 P1-21_SATA_TXP	
23	SATA_TX-	7,15 P1-23_SATA_TXN	
25	TMDS_DDC_SCL	6 P1-25_TMDS_DDC_SCL	
27	SATA_RX+	7,15 P1-27_SATA_RXP	
29	SATA_RX-	7,15 P1-29_SATA_RXN	
31	TMDS_DDC_SDA	6 P1-31_TMDS_DDC_SDA	
33	LVDS_CLK0+	6 P1-33_LVDS_CLKP	
35	LVDS_CLK0-	6 P1-35_LVDS_CLKN	
37	GND3		
39	LVDS_TX0+	6 P1-39_LVDS_P0	
41	LVDS_TX0-	6 P1-41_LVDS_N0	
43	I2C2_SCL	5,8 P1-43_I2C2_SCL	
45	LVDS_TX1+	6 P1-45_LVDS_P1	
47	LVDS_TX1-	6 P1-47_LVDS_N1	
49	I2C2_SDA	5,8 P1-49_I2C2_SDA	
51	LVDS_TX2+	6 P1-51_LVDS_P2	
53	LVDS_TX2-	6 P1-53_LVDS_N2	
55	GND4		
57	LVDS_TX3+	6,15 P1-57_LVDS_P3	
59	LVDS_TX3-	6 P1-59_LVDS_N3	
61	SDCARD_CD	4 P1-61_MMC0_CD	
63	SPI_SOMI	8 P1-63_SPI_SOMI	
65	SPI_SIMO	8 P1-65_SPI_SIMO	
67	SDCARD_WP	4 P1-67_MMC0_WP	
69	SPI_CLK	8,14 P1-69_SPI_CLK	
71	GND5		
73	PWM	5,14 P1-73_PWM	
75	GPIO3	8 P1-75_GPIO3	
77	PCAM_DAT4	9 P1-77_PCAM_DAT4/100DIFF_1P	
79	PCAM_DAT5	9 P1-79_PCAM_DAT5/100DIFF_1N	
81	PCAM_SHUTTER	9 P1-81_PCAM_SHUTTER	
83	PCAM_DAT6	9 P1-83_PCAM_DAT6/100DIFF_2P	
85	PCAM_DAT7	9 P1-85_PCAM_DAT7/100DIFF_2N	
87	GND6		
89	PCAM_DAT2	9 P1-89_PCAM_DAT2/100DIFF_3N	
91	PCAM_DAT3	9 P1-91_PCAM_DAT3/100DIFF_3P	
93	PCAM_STROBE	9 P1-93_PCAM_STROBE	
95	PCAM_PCLK	9 P1-95_PCAM_PCLK/100DIFF_4N	
97	PCAM_WEN	9 P1-97_PCAM_WEN/100DIFF_4P	
99	PCAM_RESET	9 P1-99_PCAM_RESET	
101	PCAM_DAT0	9 P1-101_PCAM_DAT0/100DIFF_5N	
103	PCAM_DAT1	9 P1-103_PCAM_DAT1/100DIFF_5P	
105	GND7		
107	PCAM_DAT8	9 P1-107_PCAM_DAT8/100DIFF_6N	
109	PCAM_DAT9	9 P1-109_PCAM_DAT9/100DIFF_6P	
111	UARTDBG_TX	4,13 P1-111_UARTDBG_TX	
113	PCAM_VSYNC	9 P1-113_PCAM_VSYNC/100DIFF_7P	
115	PCAM_HSYNC	9 P1-115_PCAM_HSYNC/100DIFF_7N	
117	UARTDBG_RX	4,13 P1-117_UARTDBG_RX	
119	PCIE_REFCLK+	7,12,17 P1-119_PCIE_REFCLKP	
121	PCIE_REFCLK-	7,12,17 P1-121_PCIE_REFCLKN	
123	GND8		
125	PCIE_TX+	7,12 P1-125_PCIE_TXP	
127	PCIE_TX-	7,12 P1-127_PCIE_TXN	
129	I2C3_SCL	R117 0R P1-129_I2C3_SCL	4,9,11,13,14 CARRIER_I2C_SCL_VPER
131	PCIE_RX+	7,12 P1-131_PCIE_RXP	
133	PCIE_RX-	7,12 P1-133_PCIE_RXN	
135	I2C3_SDA	R118 0R P1-135_I2C3_SDA	4,9,11,13,14 CARRIER_I2C_SDA_VPER
137	I2S1_CLKX	8 P1-137_I2S1_CLKX	
139	I2S1_DOUT	8 P1-139_I2S1_DOUT	
141	GND9		
143	I2S1_DIN	8 P1-143_I2S1_DIN	
145	I2S1_FSX	8 P1-145_I2S1_FSX	
147	SDIO_CMD	8 P1-147_SDIO_CMD	
149	SDIO_DAT3	8 P1-149_SDIO_DAT3	
151	SDIO_DAT2	8 P1-151_SDIO_DAT2	
153	SDIO_DAT1	8 P1-153_SDIO_DAT1	
155	SDIO_DAT0	8 P1-155_SDIO_DAT0	
157	SDIO_CLK	8 P1-157_SDIO_CLK	
159	GND10		
161	GPIO4	8,13,14 P1-161_GPIO4	
163	GPIO5	8,13 P1-163_GPIO5	
165	PWRON	9 P1-165_PWRON	
167		8,17 P1-167	
169		8,17 P1-169	
171	COLD_RESET_IN	9 P1-171_COLD_RESET_IN	
173		8,17 P1-173	
175		8,17 P1-175	
177	GND11		
179	RESERVED2	8,14 P1-179_RESERVED2	
181	RESERVED3	13,14,15 P1-181_RESERVED3	
183	BACKUP_BAT	10 P1-183_BKBAT	
185	ALT_BOOT	3,9,12,14 P1-185_ALT_BOOT	
187	nRESET_WARM	8 P1-187_nRESET_WARM	
189	EEPROM_WP	9 P1-189_EEPROM_WP	
191	ANALOG_MICBIAS/MICIN+	4 P1-191_MICBIAS	
193	ANALOG_MICIN/MICIN-	4 P1-193_MICIN	
195	AUDIO_GND	4 AGND	
197	ANALOG_RIN	4 P1-197_RLINEIN	
199	ANALOG_LIN	4 P1-199_LLINEIN	
201	ANALOG_ROUT	4 P1-201_RHPOUT	
203	ANALOG_LOUT	4 P1-203_LHPOUT	

BOTTOM

2	VCC_CM		
4	3V3A_ETH_PHY	ETH_LED2_ACT	P1-4_ETH_LED2_ACT 9
6	MDI0-/TX-		P1-6_ETH_MDI0N 9
8	MDI0+/TX+		P1-8_ETH_MDI0P 9
10	VSYS1		
12	MDI1-/RX-		P1-12_ETH_MDI1N 9
14	MDI1+/RX+		P1-14_ETH_MDI1P 9
16	ETH_LED1_SPD		P1-16_ETH_LED1_SPD 9
18	MDI2-		P1-18_ETH_MDI2N 9
20	MDI2+		P1-20_ETH_MDI2P 9
22	ETH_LED3		P1-22_ETH_LED3 9
24	MDI3-		P1-24_ETH_MDI3N 9
26	MDI3+		P1-26_ETH_MDI3P 9
28	VSYS2		
30	TMDS_CLK+		P1-30_TMDS_CLKP 6,15
32	TMDS_CLK-		P1-32_TMDS_CLKN 6,15
34	HDMI_CEC		P1-34_HDMI_CEC 6,15
36	TMDS_DAT0+		P1-36_TMDS_D0P 6,15
38	TMDS_DAT0-		P1-38_TMDS_D0N 6,15
40	TMDS_HPD		P1-40_HDMI_HPD 6,15
42	TMDS_DAT1+		P1-42_TMDS_D1P 6,15
44	TMDS_DAT1-		P1-44_TMDS_D1N 6,15
46	VSYS3		
48	TMDS_DAT2+		P1-48_TMDS_D2P 6,15
50	TMDS_DAT2-		P1-50_TMDS_D2N 6,15
52	SPI_CS1		P1-52_SPI_CS1 8
54	GPIO8		P1-54_GPIO8 8,17
56	GPIO9		P1-56_GPIO9 8,17
58	SPI_CS0		P1-58_SPI_CS0 8,14
60	GPIO10		P1-60_GPIO10 4,8
62	GPIO11		P1-62_GPIO11 8
64	VSYS4		
66	RTOUCH_X+		P1-66_RTOUCH_XP 5,8
68	RTOUCH_X-		P1-68_RTOUCH_XN 5,8
70	RTOUCH_Y+		P1-70_RTOUCH_YP 5,8
72	RTOUCH_Y-		P1-72_RTOUCH_YN 5,8
74	PDISP_DAT22		P1-74_PDISP_DATA22 5
76	PDISP_DAT23		P1-76_PDISP_DATA23 5
78	VSYS5		
80	SDCARD_CLK		P1-80_MMC0_CLK 4
82	SDCARD_CMD		P1-82_MMC0_CMD 4
84	SDCARD_DAT0		P1-84_MMC0_DAT0 4
86	SDCARD_DAT1		P1-86_MMC0_DAT1 4
88	SDCARD_DAT2		P1-88_MMC0_DAT2 4
90	SDCARD_DAT3		P1-90_MMC0_DAT3 4
92	PDISP_DAT17		P1-92_PDISP_DATA17 5
94	PDISP_DAT16		P1-94_PDISP_DATA16 5
96	VSYS6		
98	PDISP_PCLK		P1-98_PDISP_PCLK 5
100	PDISP_HSYNC		P1-100_PDISP_HSYNC 5
102	PDISP_VSYNC		P1-102_PDISP_VSYNC 5
104	PDISP_DE		P1-104_PDISP_DE 5
106	PDISP_DAT0		P1-106_PDISP_DATA00 5
108	PDISP_DAT1		P1-108_PDISP_DATA01 5
110	PDISP_DAT2		P1-110_PDISP_DATA02 5
112	PDISP_DAT3		P1-112_PDISP_DATA03 5
114	VSYS7		
116	PDISP_DAT4		P1-116_PDISP_DATA04 5
118	PDISP_DAT5		P1-118_PDISP_DATA05 5
120	PDISP_DAT6		P1-120_PDISP_DATA06 5
122	PDISP_DAT7		P1-122_PDISP_DATA07 5
124	PDISP_DAT8		P1-124_PDISP_DATA08 5,14
126	PDISP_DAT9		P1-126_PDISP_DATA09 5,14
128	PDISP_DAT10		P1-128_PDISP_DATA10 5,14
130	PDISP_DAT11		P1-130_PDISP_DATA11 5,14
132	VSYS8		
134	PDISP_DAT12		P1-134_PDISP_DATA12 5
136	PDISP_DAT13		P1-136_PDISP_DATA13 5
138	PDISP_DAT14		P1-138_PDISP_DATA14 5
140	PDISP_DAT15		P1-140_PDISP_DATA15 5
142	PDISP_DAT18		P1-142_PDISP_DATA18 5
144	PDISP_DAT19		P1-144_PDISP_DATA19 5
146	PDISP_DAT20		P1-146_PDISP_DATA20 5
148	PDISP_DAT21		P1-148_PDISP_DATA21 5
150	VSYS9		
152	GPIO1		P1-152_GPIO1 8,11
154	GPIO2		P1-154_GPIO2 8
156	USB_PWREN		P1-156_USBPWREN 8
158	HSUSB3_D-		P1-158_HSUSB3_DN 8
160	HSUSB3_D+		P1-160_HSUSB3_DP 8
162	USB_nOVC		P1-162_nOVC 8
164	HSUSB2_D-		P1-164_HSUSB2_DN 8,14
166	HSUSB2_D+		P1-166_HSUSB2_DP 8,14
168	VSYS10		
170	HSUSB1_D-		P1-170_HSUSB1_DN 8
172	HSUSB1_D+		P1-172_HSUSB1_DP 8
174	USBOTG_ID		P1-174_USBOTG_ID 8
176	HSUSB0_D+		P1-176_USBOTG_DP 8
178	HSUSB0_D-		P1-178_USBOTG_DN 8
180	USBOTG_VBUS		VBUS0
182	SSUSB_RX+		P1-182_USBSS_RXP 8,12
184	SSUSB_RX-		P1-184_USBSS_RXN 8,12
186	VSYS11		
188	SSUSB_TX+		P1-188_USBSS_TXP 8,12
190	SSUSB_TX-		P1-190_USBSS_TXN 8,12
192	RESERVED4		P1-192_RESERVED 11,14,15,16
194	GPIO6		P1-194_GPIO6 5,8
196	BOOT_PWR_IN		P1-196_BOOT_PWR_IN 8,13
198	PER_PWREN_OUT		P1-198_PER_PWREN_OUT 8
200	GPIO7		P1-200_GPIO7 8,14
202	PER_PWREN_REQ		P1-202_PER_PWREN_REQ 12
204	VSYS12		

VDD3A_ETH

REF PLANE STITCHING CAPACITORS

VCC_CM
C1 C2 C7 C8 C3 C4 C9 C10 C5 C6 C11 C12 C206 C207 C208 100nF
DNP

VSB_3V3_DC
C240 C241 C242 C243 C244 C245 C246 C247 C248 C249 C250 C251 C258 C259 C260 C261 C263 C262 C264 C265 C266 C267 100nF

VSB_3V3_DC
C299 C202 C231 C230 C232 C221 C220 C223 C222 C203 C210 C211 C212 C213 C234 C233 C236 C235 C295 C296 C297 C298 100nF

C289 C292 C291 C294 C293 C290 C279 C286 C285 C288 C287 C281 C280 C282 C283 C284 C214 C225 C224 C227 C226 C215 C216 C217 C218 C219 100nF

Power Rails

3,4,5,6,7,8,9,10 CHASSIS
FB12 120 Ohm@3.5A
DNP C194 1nF/2KV

DO NOT POPULATE FOR:
SB-SOM-T54
SB-SOM-QS600

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SHIFT PARALLEL RGB TO 3.3V

NOTE: In case CoM/SoM I/O is @ 3.3V levels, such as CM-T43/CL-SOM-iMX6UL/CL-SOM-AM57x, level shifting is not required. We use level shifting here only to be compatible with non-3.3V I/O CoMs (such as CM-T54 or CM-QS600)

DO NOT POPULATE FOR: SB-SOM-QS600

Make sure DATA to COLOR mapping is valid for all CoMs compatible with SB-SOM

PARALLEL RGB LCD & TOUCH

SHENZHEN STARTEK ELECTRONIC TECHNOLOGY KD050C-1A-TP LCD

Place on board bottom

Typical LED configuration: Two parallel chains of 6 serially connected LEDs

PARALLEL RGB to LVDS

POPULATED ONLY FOR:
SB-SOM-T43
SB-SOM-iMX6UL

DS90C385A

PARALLEL RGB-to-DVI

STRAPS:
Without I2C:
1. Monitor detection through MSEN
2. 24bit input mode
3. RGB data latched on rising PCLK edge
4. De-skewing is set to 0b001 (-0.9nS <-> -0.75 nS)

With I2C: Full SW control

Assemble for NON I2C config

Assemble for I2C config

7-bit I2C address: 0b011,1001

DO NOT POPULATE FOR: SB-SOM-QS600

Circuitry is designed to shift DDC signals logic levels between VSB_PER (1.8 or 3.3V) and 5V.

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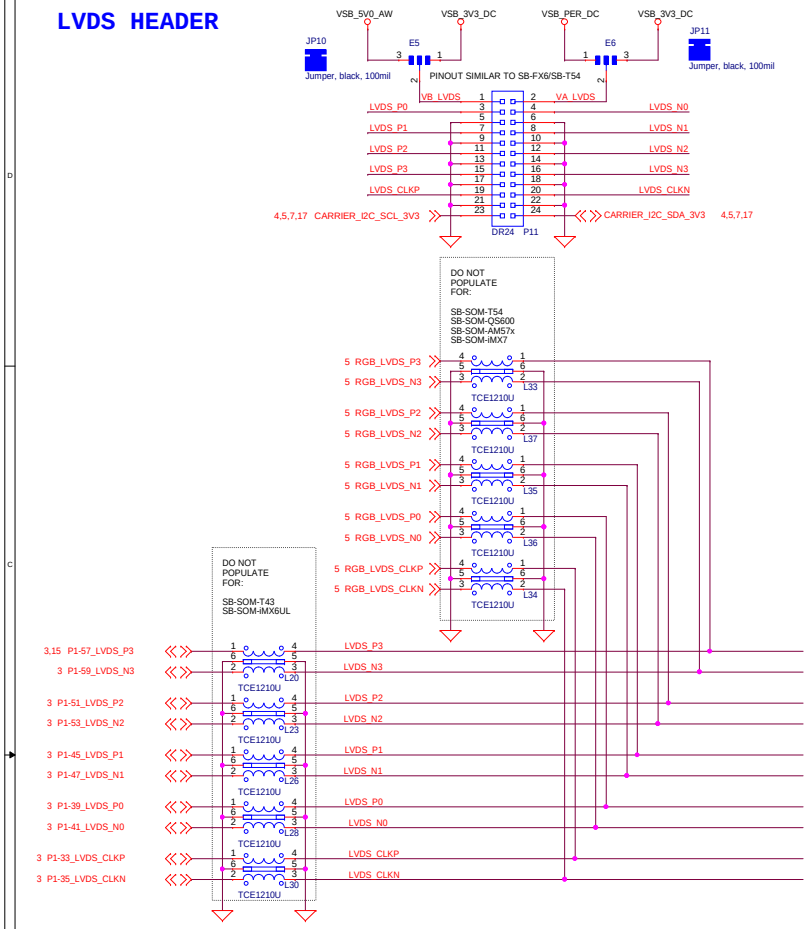
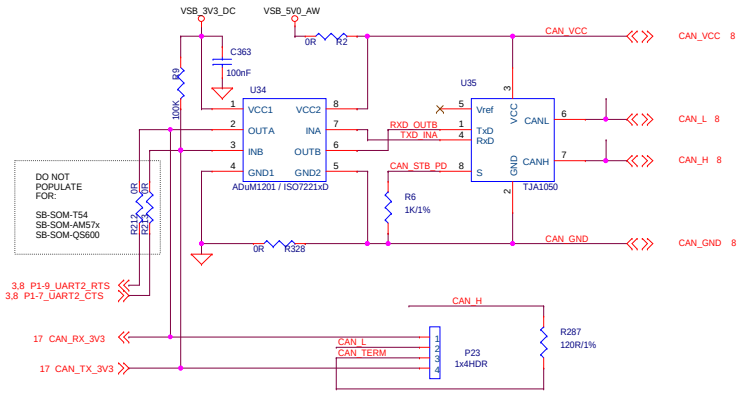
LVDS HEADER

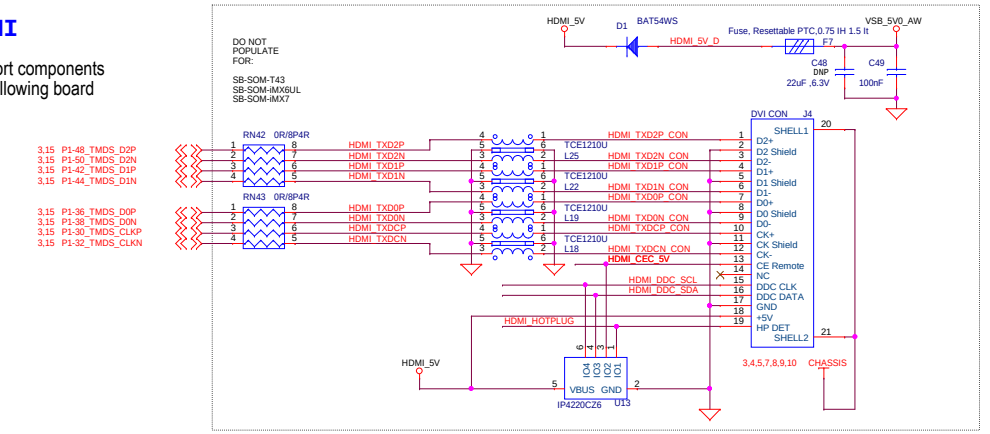


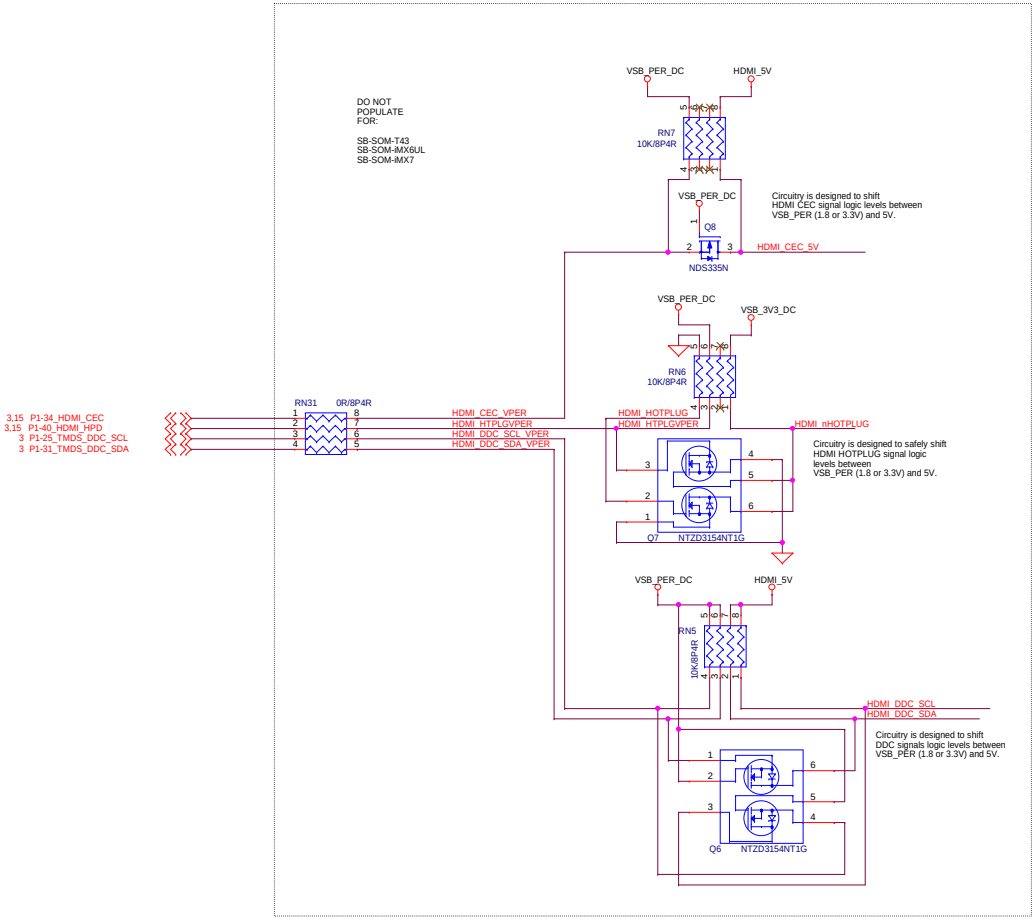
CAN TRANSCEIVER
(not populated with SB-SOM-T54 and SB-SOM-QS600)



SoM NATIVE HDMI

NOTE: The native HDMI port components are not populated for the following board configurations:
SB-SOM-iMX6UL*
SB-SOM-T43*





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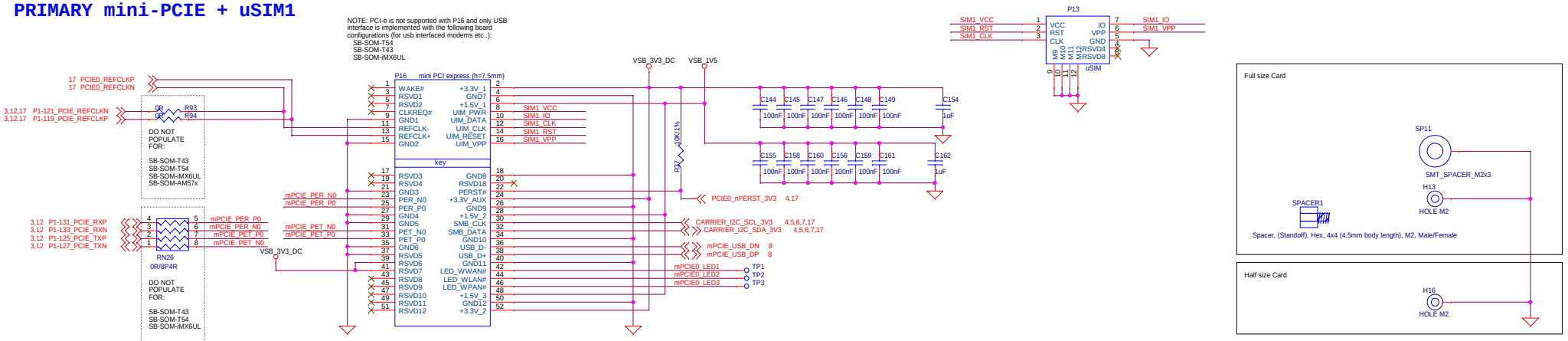
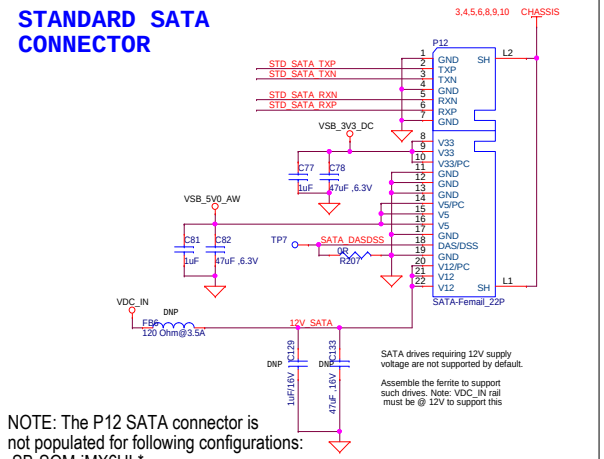
PRIMARY mini-PCIE + uSIM1

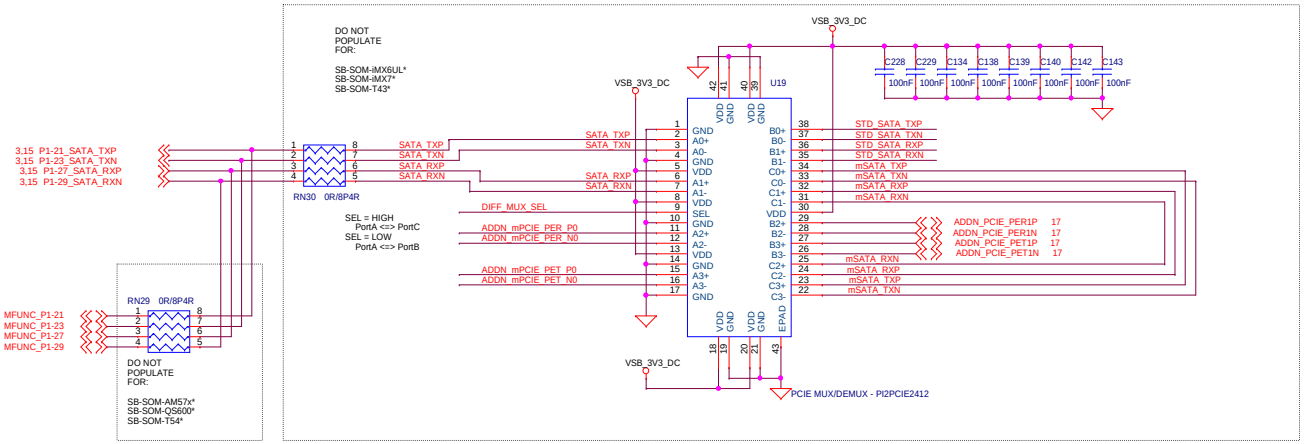


STANDARD SATA CONNECTOR



NOTE: The P12 SATA connector is not populated for following configurations:
SB-SOM-iMX6UL*
SB-SOM-iMX7*
SB-SOM-T43*

PCIE/SATA/mSATA MUX

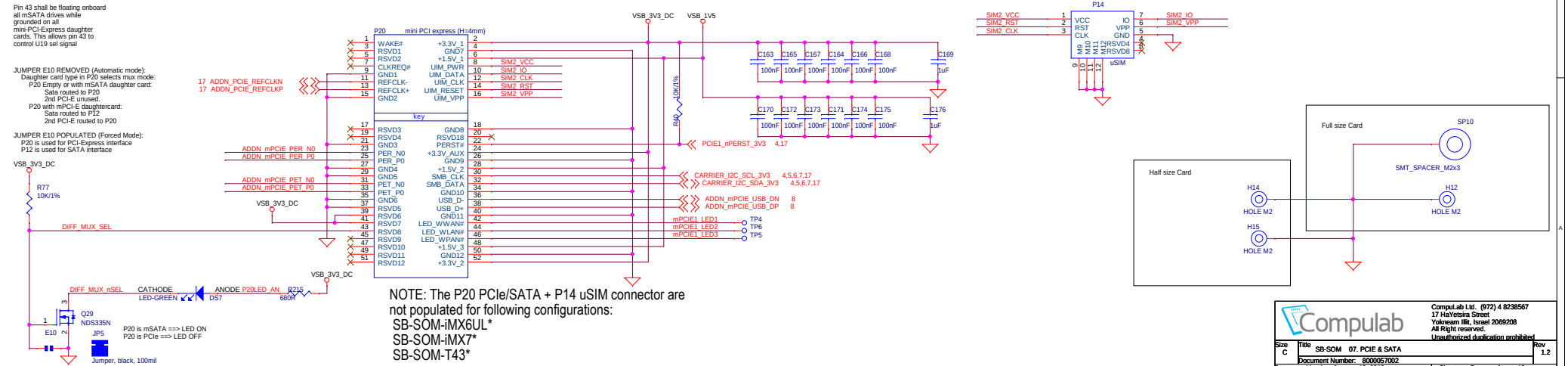


SECONDARY PCIE/mSATA/USB + uSIM2

Pin 43 shall be floating onboard all mSATA drives while grounded on all mini-PCI-Express daughter cards. This allows pin 43 to control U19 sel signal

JUMPER E10 REMOVED (Automatic mode):
Daughter card type in P20 selects mux mode:
P20 Empty or with mSATA daughter card:
Sata routed to P20
2nd PCI-E unused.
P20 with mPCI-E daughtercard:
Sata routed to P12
2nd PCI-E routed to P20

JUMPER E10 POPULATED (Forced Mode):
P20 is used for PCI-Express interface
P12 is used for SATA interface



NOTE: The P20 PCIe/SATA + P14 uSIM connector are not populated for following configurations:
SB-SOM-iMX6UL*
SB-SOM-iMX7*
SB-SOM-T43*

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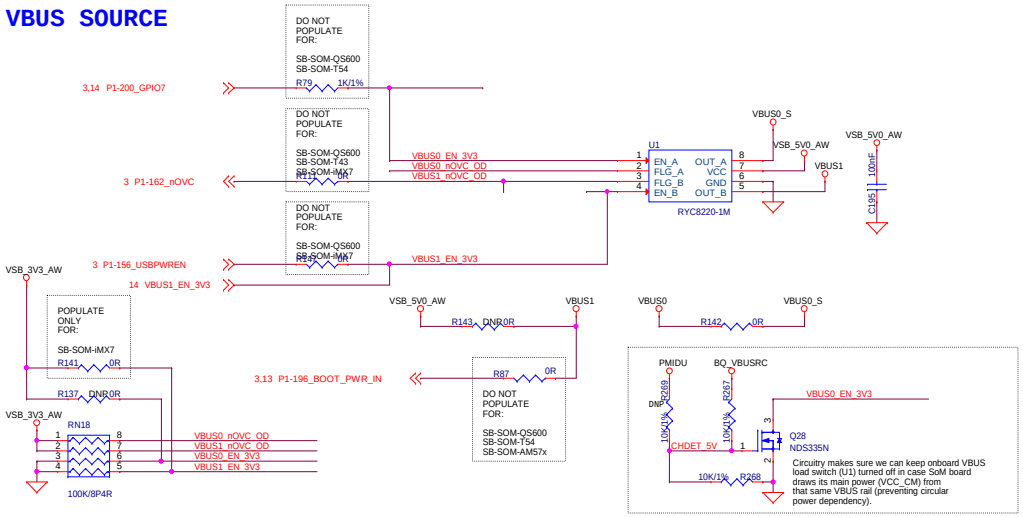
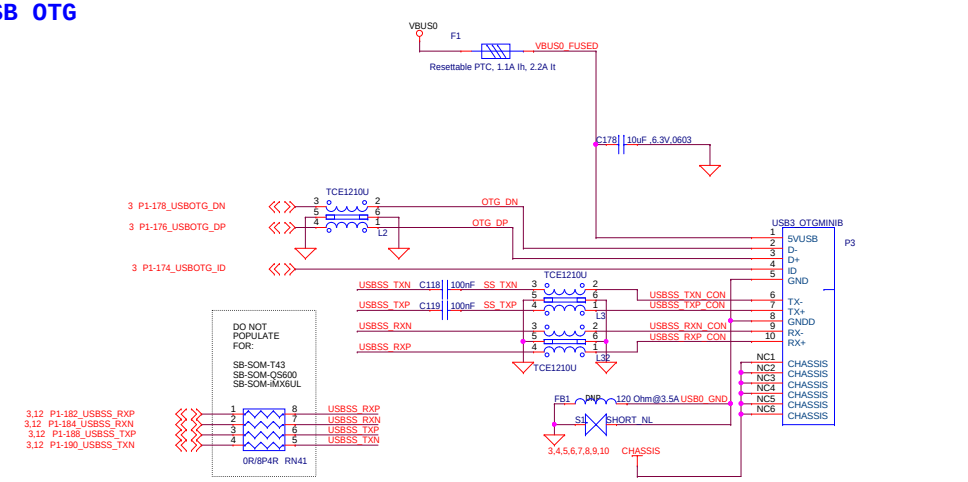
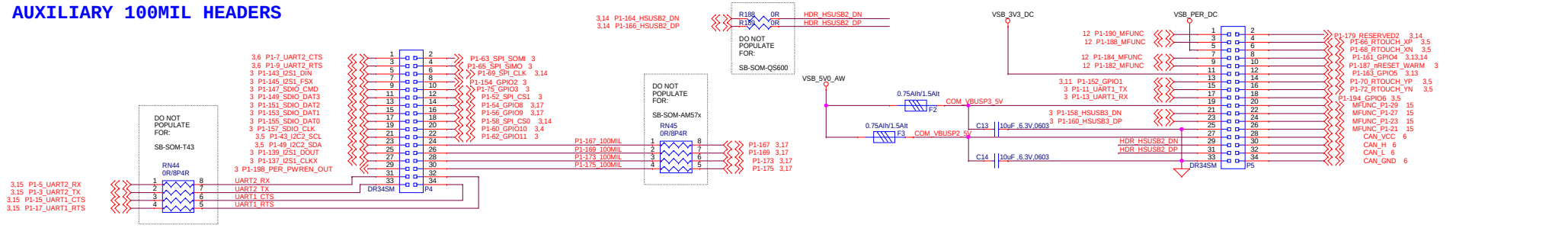
VBUS SOURCE



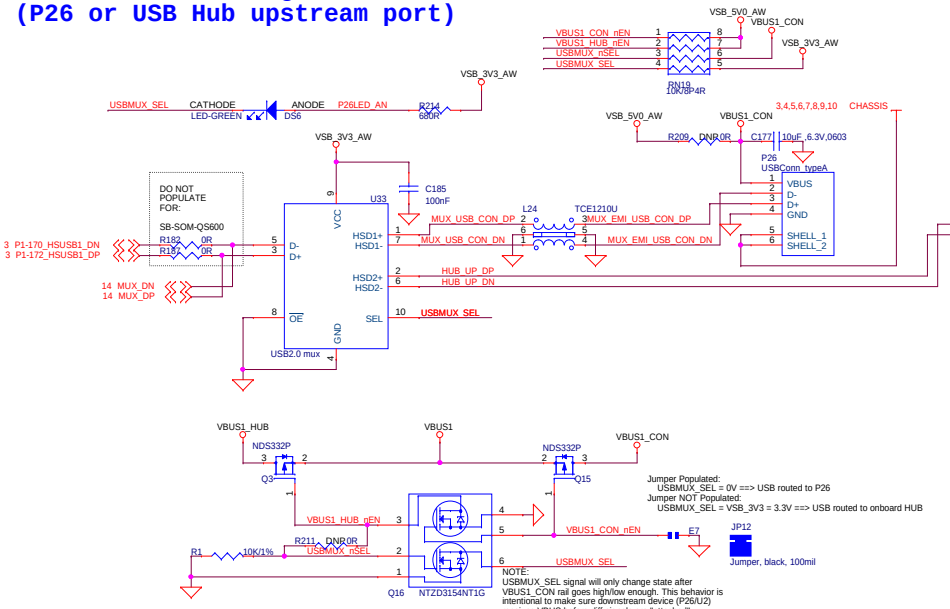
USB OTG



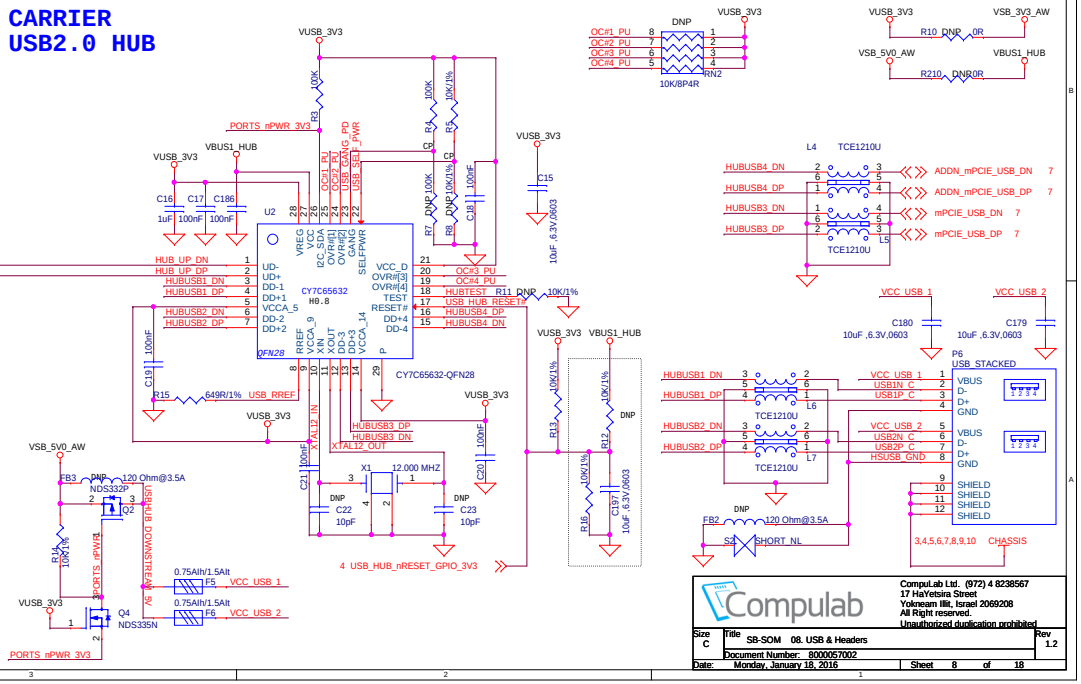
AUXILIARY 100MIL HEADERS



SoM/CoM USB2.0 usage selecor (P26 or USB Hub upstream port)



CARRIER USB2.0 HUB



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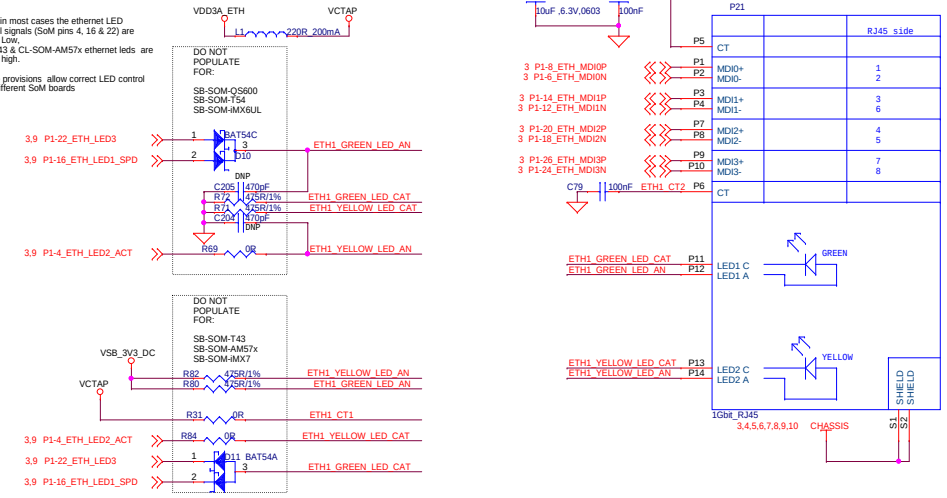
PRIMARY CoM/SoM ETHERNET RJ45

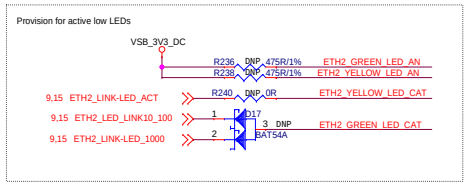
While in most cases the ethernet LED control signals (SoM pins 4, 16 & 22) are active Low,
CM-T43 & CL-SOM-AM57x ethernet leds are active high.

These provisions allow correct LED control with different SoM boards



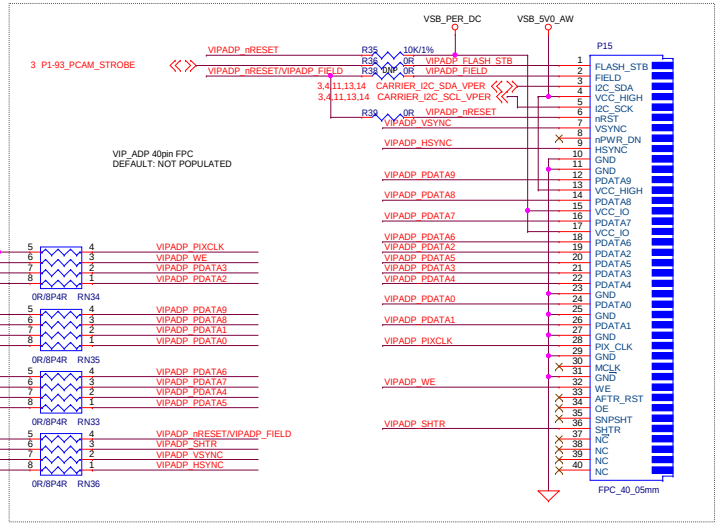
SECONDARY ETHERNET RJ-45

Can be utilized only with following SoM + Carrier Combinations:
1. Stock CM-T43 + SB-SOM-T43 --> LEDs active high

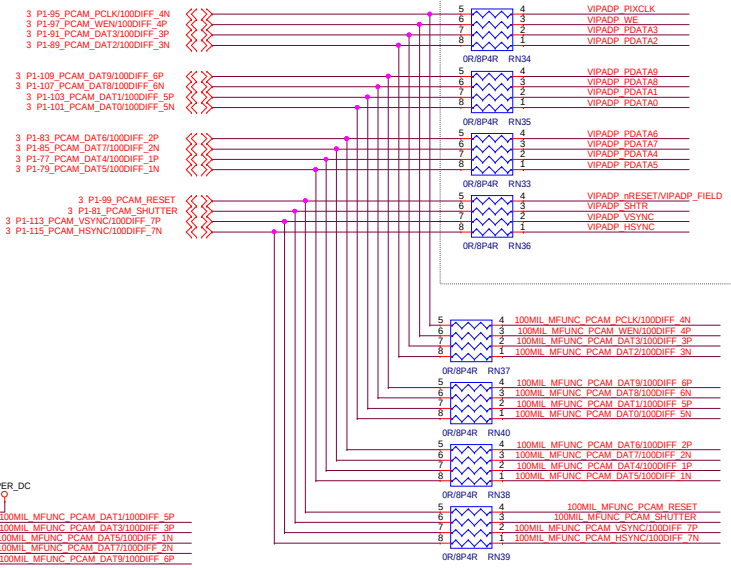


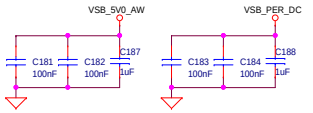
NOTE: The secondary ethernet RJ-45 is not populated for following configurations:
SB-SOM-QS600*
SB-SOM-AM57x*
SB-SOM-iMX6UL*
SB-SOM-T54*

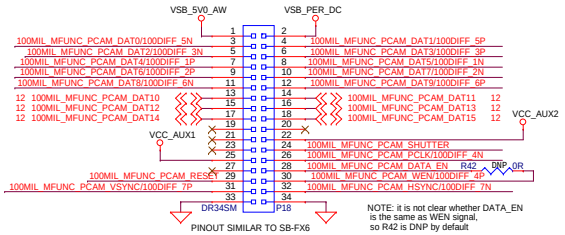
PARALLEL CAMERA INTERFACE OPTIONS



VIP_ADP 40pin FPC
DEFAULT: NOT POPULATED





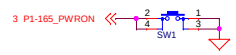


PINOUT SIMILAR TO SB-FX6

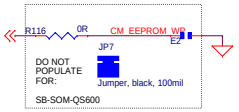
NOTE: it is not clear whether DATA_EN is the same as WEN signal, so R42 is DNP by default

POWER/RESET/BOOT SWITCHES

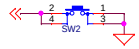
Active low power button input to SoM:
Signal pulled high onboard SoM. SoM behavior may differ with different SoMs. Please refer to SoM specific reference manual for detailed information.

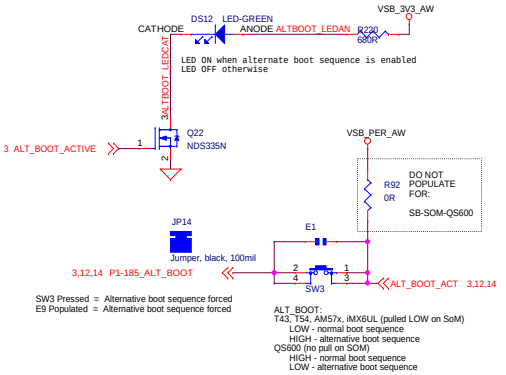


SoM onboard EEPROM write protection feature:
Signal pulled high onboard SoM. SoM behavior may differ with different SoMs. Please refer to SoM specific reference manual for detailed information.



SoM active low reset button input to SoM:
SoM behavior may differ with different SoMs. Please refer to SoM specific reference manual for detailed information.





SW3 Pressed = Alternative boot sequence forced
E9 Populated = Alternative boot sequence forced

ALT_BOOT:
T43, T54, AM57x, iMX6UL (pulled LOW on SoM)
LOW - normal boot sequence
HIGH - alternative boot sequence
QS600 (no pull on SOM)
HIGH - normal boot sequence
LOW - alternative boot sequence

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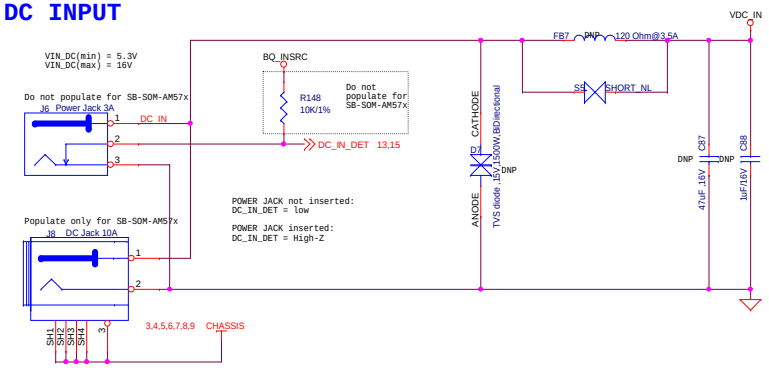
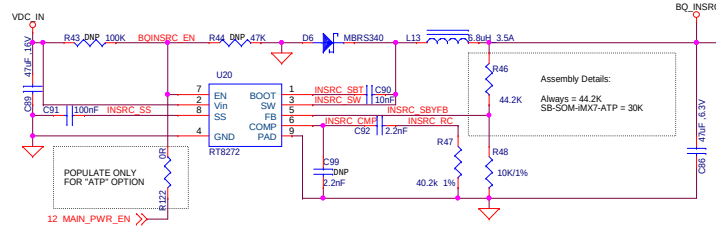
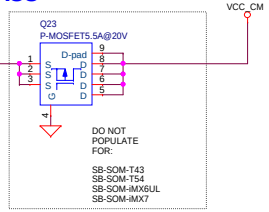
DC INPUT



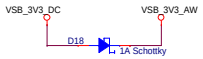
DC-to-5.25V



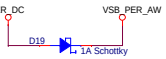
CHARGER BYPASS



VSB_3V3_AW SOURCE (FROM DC)

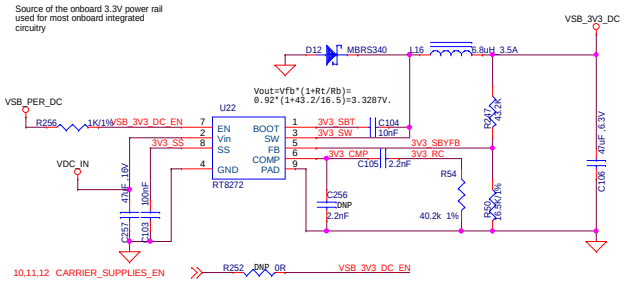


VSB_PER_AW SOURCE (FROM DC)

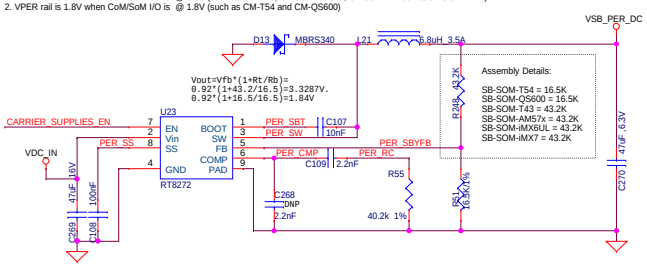


VSB_5V0_AW SOURCE (FROM DC)

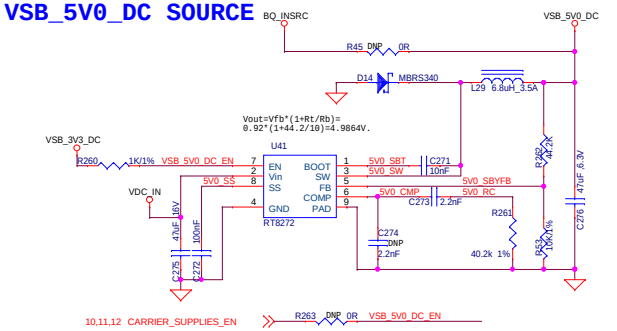
VSB_3V3_DC SOURCE



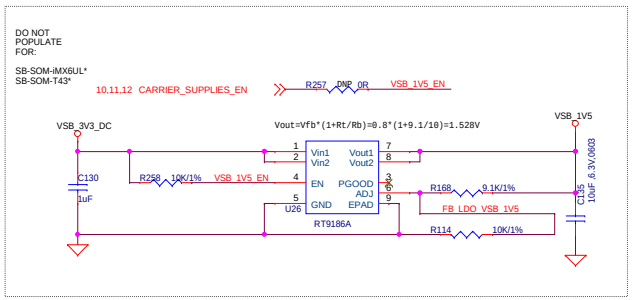
VSB_PER_DC SOURCE



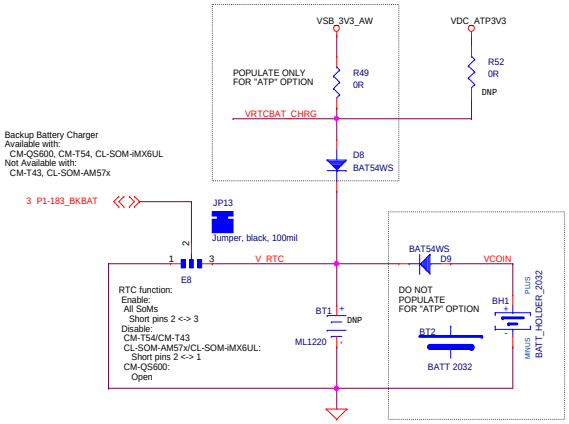
VSB_5V0_DC SOURCE



1V5 SOURCE FOR PCI-e (enabled only when main power source is DC)



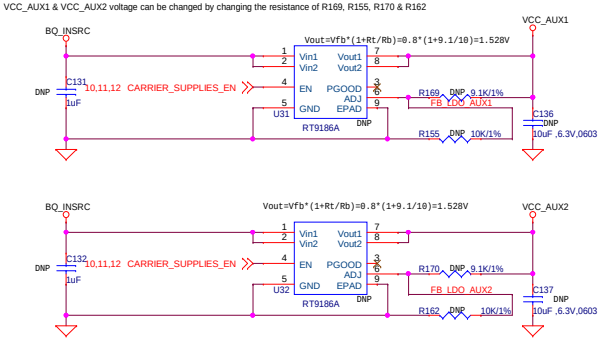
RTC BATTERY



VCC_AUX1 & VCC_AUX2 sources NOT POPULATED BY DEFAULT

These placeholders allow generating additional voltages rails often required by different camera sensors.
The VCC_AUX1 & VCC_AUX2 voltages can be sourced into the sensor from the 100mil camera header

VCC_AUX1 & VCC_AUX2 voltage can be changed by changing the resistance of R169, R155, R170 & R162



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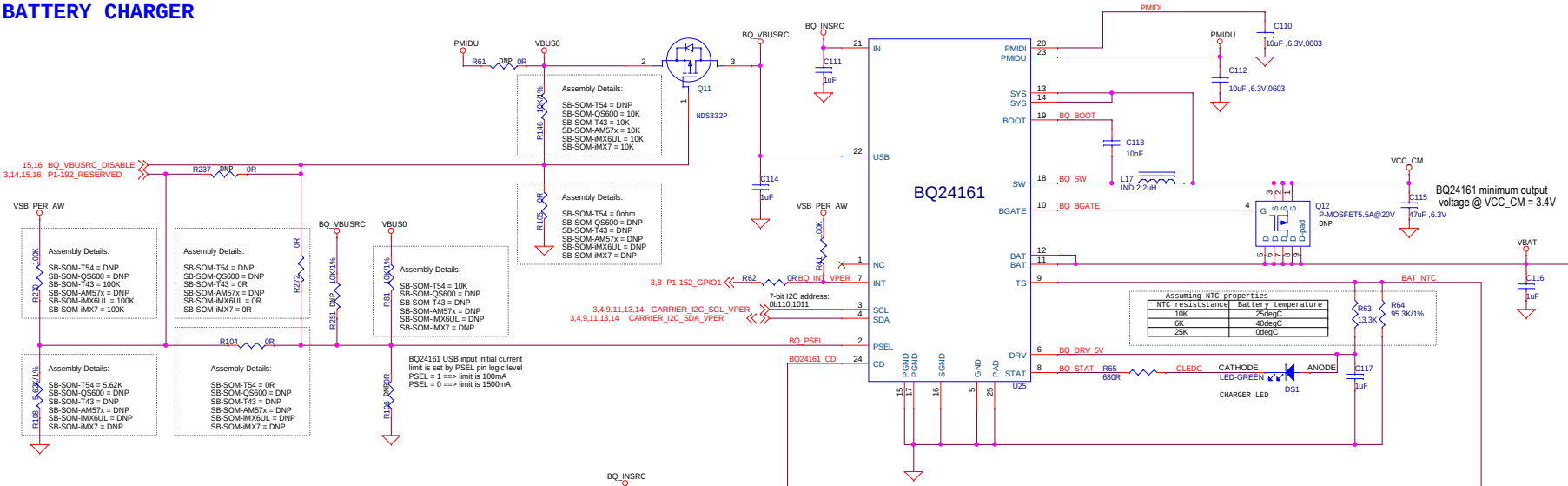
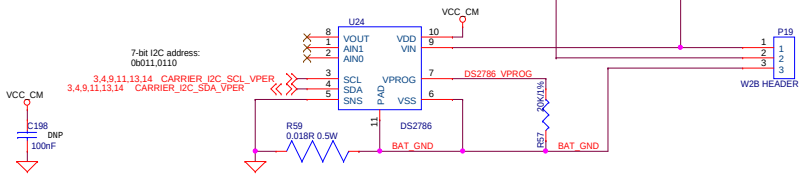
AUTOMATIC POWER SOURCE SWITCHING BETWEEN BATTERY / DC / USB-OTG PORT. & BATTERY CHARGER



NOTE: U21, U24, U25 U38, U39 and their preipherals are not populated with ATP configurations and the following non-ATP configurations:
SB-SOM-QS600
SB-SOM-AM57x

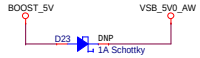
Li-Po Battery Connector & Charging supervisor



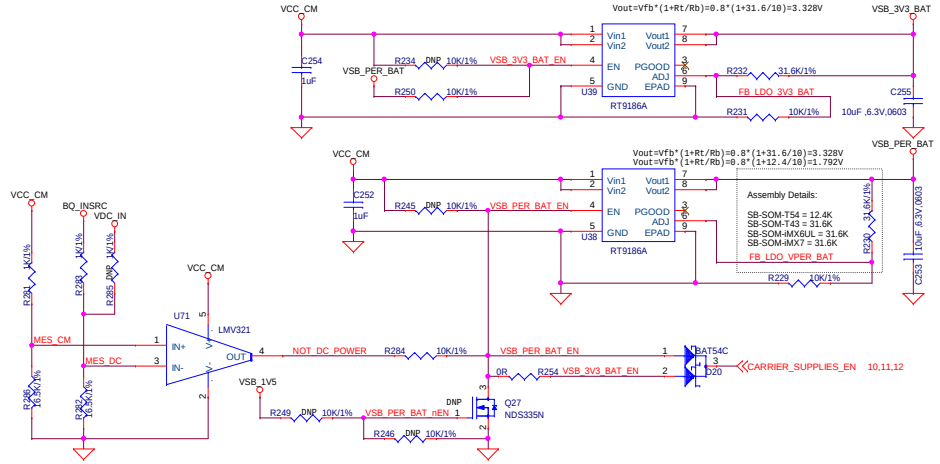
VSB_PER_AW SOURCE (FROM BATTERY/USB)

VSB_3V3_AW SOURCE (FROM BATTERY/USB)

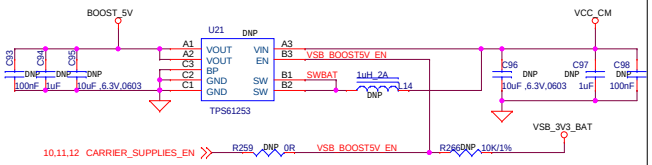
VSB_5V0_AW SOURCE (FROM BATTERY/USB)



VSB_PER_BAT & VSB_3V3_BAT sources



5V SOURCE FROM BATTERY (PROVISION)



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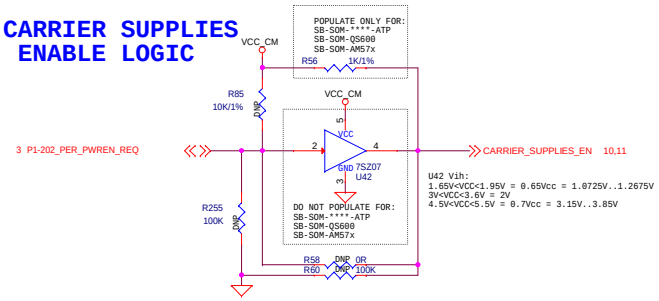
CARRIER SUPPLIES ENABLE LOGIC

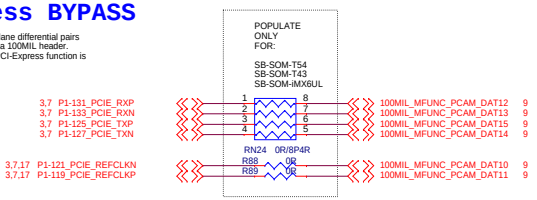


U42 Vih:
1.65V<VCC<1.95V = 0.65Vcc = 1.0725V..1.2675V
3V<VCC<3.6V = 2V
4.5V<VCC<5.5V = 0.7Vcc = 3.15V..3.85V

T54: CM-T54 drives this P1-202 high (VCC_CM) as part of powering-up.
CM-T43: A standard GPIO is exposed through P1-202. By default the GPIO is pulled up to 3.3V onboard CM-T43.
SW should drive low here when CM-T43 is in low power modes to disable carrier board supplies.
CM-QS600: We do not support low power modes with SB-SOM-QS600. Remove U42, R58 and R60 to always keep carreir board power supplies enabled.
CL-SOM-AM57x: We do not support low power modes with SB-SOM-AM57x. Remove U42, R58 and R60 to always keep carreir board power supplies enabled.
CL-SOM-iMX6UL: i.MX6UL drives P1-202 low as soon as it enters low power mode. This signal is pulled trough 100K to 3.3V onboard CL-SOM-iMX6UL
CL-SOM-iMX7: i.MX7 drives P1-202 low as soon as it enters low power mode. This signal is pulled trough 100K to 3.0V onboard CL-SOM-iMX7

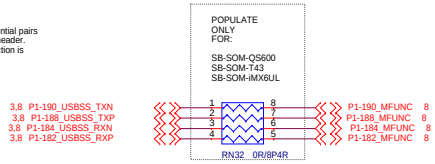
PCI-Express BYPASS

Allows using the PCI-Express lane differential pairs for alternate functions through a 100MIL header. Useful with CoM/SoM where PCI-Express function is not available

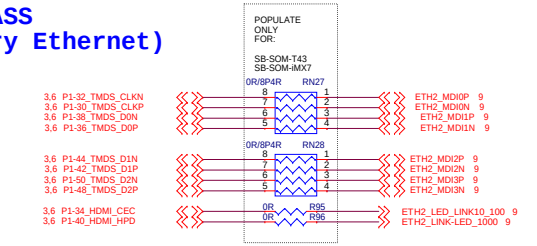


USB3.0 BYPASS

Allows using the USB 3.0 RX & TX differential pairs for alternate functions through a 100MIL header. Useful with CoM/SoM where USB3.0 function is not available



HDMI BYPASS (Secondary Ethernet)



USB CHARGER LOGIC (iMX6UL / iMX7)

DO NOT POPULATE BY DEFAULT!

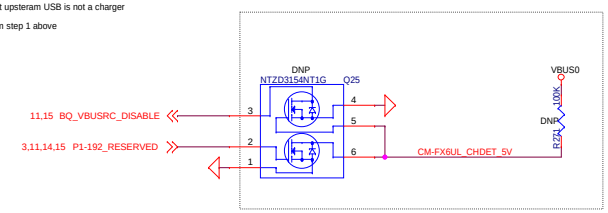
CL-SOM-iMX6UL / CL-SOM-iMX7 should drive the P1-192_RESERVED open drain signal LOW whenever a USB charger is connected (and detected) to P3 USB OTG connector. P1-192 is only 3.3V tolerant. Please refer to respective SOM hardware reference manual for additional details.

This circuitry allows SBC-iMX6UL / SBC-iMX7 to source VCC_CM (main power rail for SoM) from VBUS0 rail upon detection of a USB charger on P3 connector (USB OTG).

No DC Power & Dead Battery (only power source is USB) case:

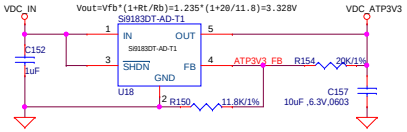
Since BQ24161 USB power input is open by default (allowing BQ24161 to source VCC_CM from VBUS0). system will be able to start from USB charger on P3.
The drawback here, is that when a VBUS0 is generated from a simple upstream USB host port (not a charger), the system would constantly try to start, until a chrager is connected to P3 with the following infinite loop:

1. Start
2. Detect that upsteram USB is not a charger
3. Power-off
4. repeat from step 1 above



PRODUCTION SPECIFIC PROVISIONS not assembled by default

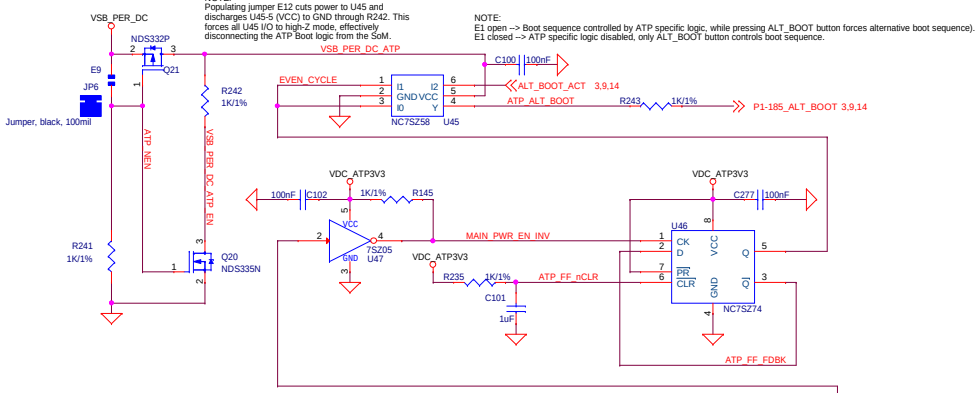
Production power rail - always on



Boot sequence auto-toggle logic

NOTE:
Populating jumper E12 cuts power to U45 and discharges U45-5 (VCC) to GND through R242. This forces all U45 I/O to high-Z mode, effectively disconnecting the ATP Boot logic from the SoM.

NOTE:
E1 open --> Boot sequence controlled by ATP specific logic, while pressing ALT_BOOT button forces alternative boot sequence).
E1 closed --> ATP specific logic disabled, only ALT_BOOT button controls boot sequence.



Board power-cycle logic

Boardwide power Cycle is triggered by a low, 1uS (min) pulse on the MAIN_PWR_CYCLE signal

U37 is an optional oneshot circuitry can only be used in case Q17 is not populated

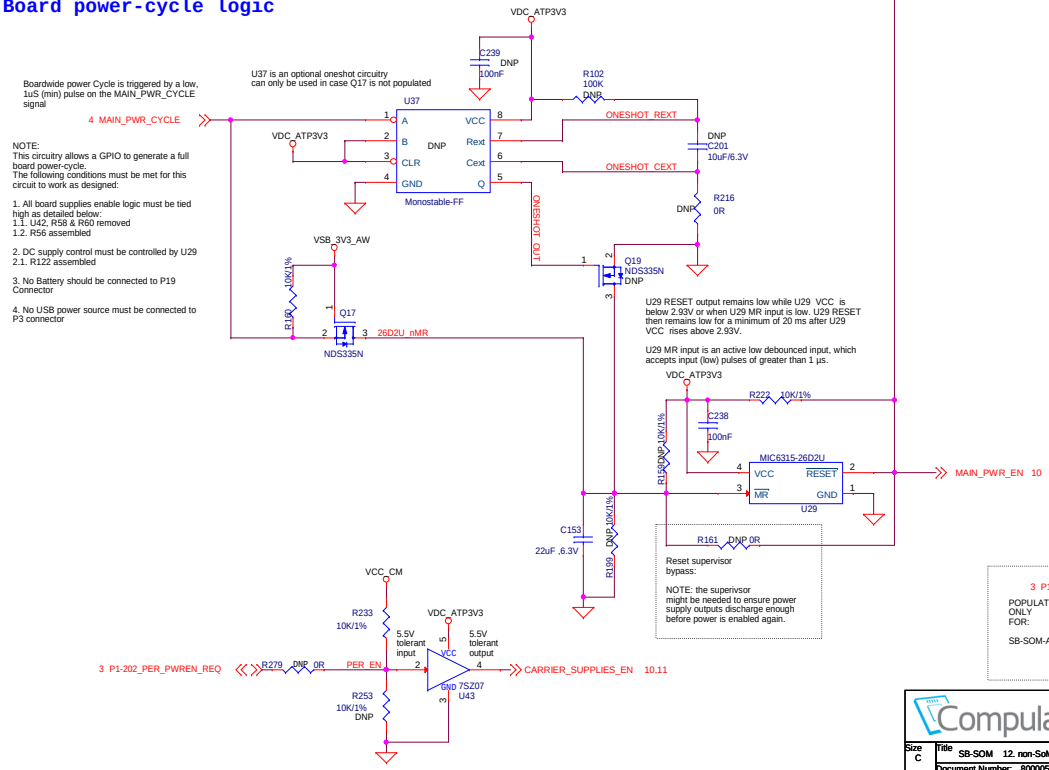
NOTE:
This circuitry allows a GPIO to generate a full board power-cycle.
The following conditions must be met for this circuit to work as designed:

1. All board supplies enable logic must be tied high as detailed below:
1.1. U42, R58 & R60 removed
1.2. R56 assembled

2. DC supply control must be controlled by U29
2.1. R122 assembled

3. No Battery should be connected to P19 Connector

4. No USB power source must be connected to P3 connector



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Size	Title	Rev
C	SB-SOM 12. non-SoM-Specific bypass	1.2
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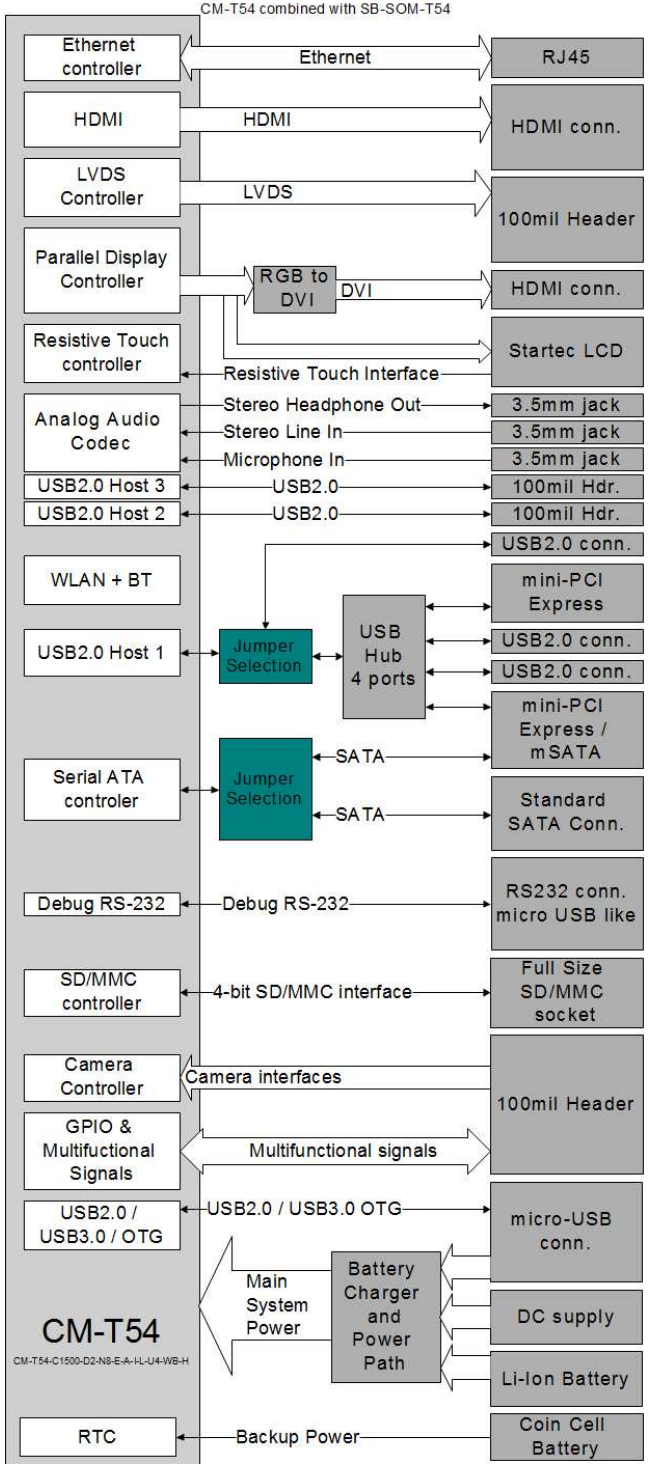
SBC2-T54

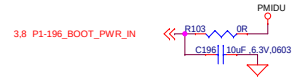
CM-T54 combined with SB-SOM-T54



SB-SOM-T54 Specific Provisions
Populated only for SB-SOM-T54

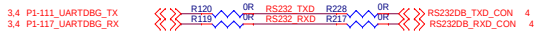
SB-SOM-T54 PRIMARY POWER from USB-OTG

Allows CM-T54 to operate from VBUS0 (overcoming the initial 100mA current limit of USB), as described in CM-T54 reference manual chapter 5.5



SB-SOM-T54 PRIMARY I2C BUS

SB-SOM-T54 PRIMARY DEBUG UART/RS-232



SB-SOM-T54 I2C USED FOR DVI DDC

SB-SOM-T54 AC-Adapter detection

```
P1-181 = VAC_DETECT

VAC_DETECT Default settings:
1. VAC_OK ON request is registered by CM-T54
upon rising of VAC_DETECT voltage above 3.6V(max),
or falling of VAC_DETECT voltage below 2.8V(min)
2. In case VCC_CM & BACKUP Battery are not available
while VAC_DETECT rises above 3.6V(max), CM-T54
transitions from "NO SUPPLY" power state
to "BACKUP" power state.
3. This CM-T54 input is tolerant to voltages between 0V & 10V
```

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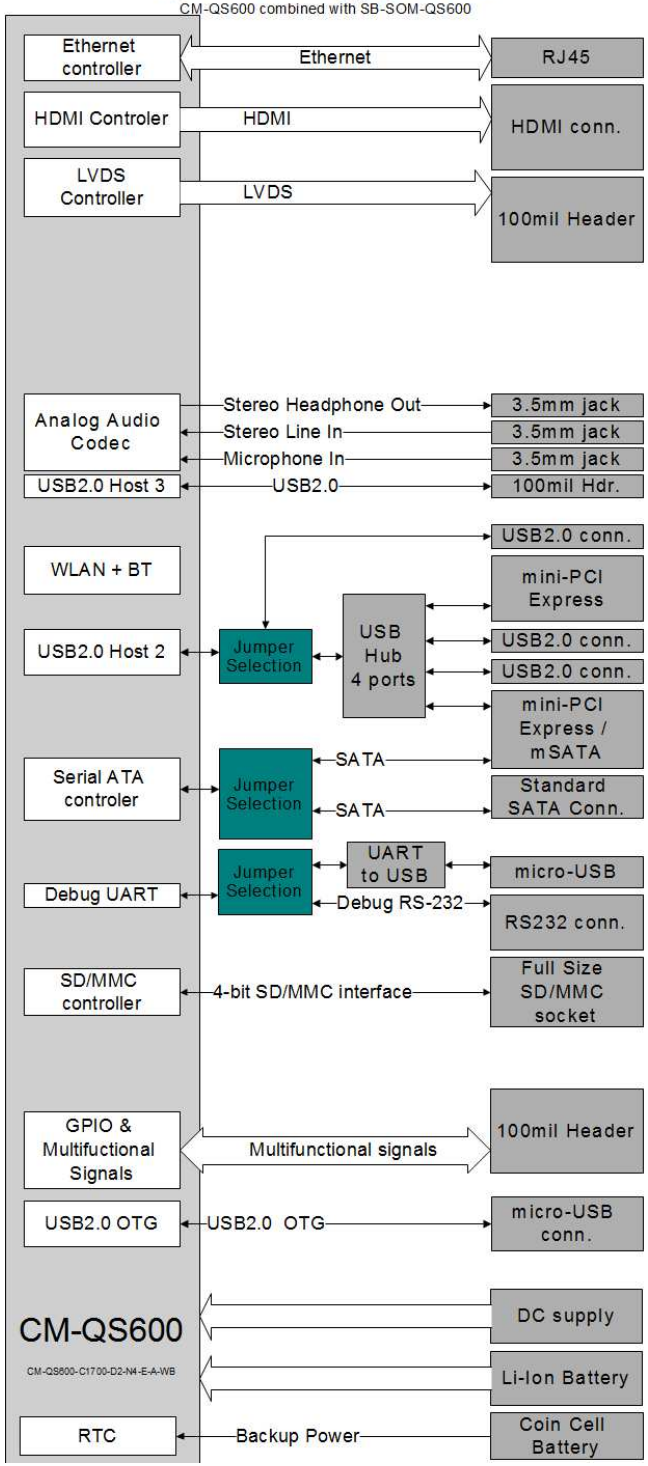
SBC2-QS600

CM-QS600 combined with SB-SOM-QS600



SB-SOM-QS600 Specific Provisions
Populated only for SB-SOM-QS600

SB-SOM-QS600 USB HOST POWER CONTROL

SB-SOM-XXX uses the 3.3V USBPWR_EN function on pin 156 of SoM/CoM interface to enable VBUS (VBUS1 rail) for the USB Hub / P26 USB conenctor (page8). Using pin 156 with SB-SOM-QS600 is not possible since a 3.3V signal is required to enable VBUS1, while a 1.8V GPIO is routed to pin 156 onboard CM-QS600.

To overcome this, we are using pin 200 of CM-QS600 interface, (which has 3.3V GPIO functionality with all CM-QS600 configurations), with SB-SOM-QS600, allowing VBUS1 control by means of 3.3V GPIO.

3,8 P1-200_GPIO7 — R149 0R — VBUS1_EN_3V3 8

SB-SOM-QS600 USB Hub upstream port

Normally, SB-SOM-XXX uses the SoM USB2.0 port on pins 170 & 172 as the upstream USB port of the carrier USB Hub (page8). CM-QS600 does not implement a USB2.0 interface on pins 170 & 172.

To overcome this, we are using the USB port CM-QS600 implements on pins 164 & 166 as the upstream USB port of SB-SOM-QS600 USB Hub

3,8 P1-164_HSUSB2_DN — R190 0R — MUX_DN 8
3,8 P1-166_HSUSB2_DP — R191 0R — MUX_DP 8

CM-QS600 BOOT STRAPS & SEQUENCES

Normal Boot sequence:
1st device: CM-QS600 onboard eMMC.
2nd device: None

Alternate Boot Sequence:
1st device: SD card in SB-SOM-QS600 full size SD slot
2nd device (if bootloader not found in first device): CM-QS600 onboard eMMC.

P1-124_PDISP_DATA08 3,5
P1-126_PDISP_DATA09 3,5
P1-128_PDISP_DATA10 3,5
P1-130_PDISP_DATA11 3,5
10K/8P4R RN23

3,5 P1-73_PWM
P1-179_RESERVED2 3,8
P1-181_RESERVED3 3,13,15
0R/8P4R RN25

VSB_PER_AW
R144 0R QS600_GPIOBTN R107 10K/1%
SW4 Low profile switch

VSB_PER_AW
3,9,12 P1-185_ALT_BOOT — R90 10K/1%

NOTE:
While the ALT_BOOT signal logic of most CoM/SoMs is as follows:
Z or 0 ==> Normal Boot Sequence
1 ==> Alternate Boot Sequence
CM-QS600 ALT_BOOT signal logic is inverted as shown below:
0 ==> Alternate Boot Sequence.
1 ==> Normal boot sequence.

R91 0R — ALT_BOOT_ACT 3,9,12

NOTE:
By default, P1-73 is a GPIO sensed by CM-QS600 fastboot firmware. In case this signal is low, fastboot SW does not move forward with CM-QS600 boot process, it stops and communicates with host PC through USB port P3. Press SW4 to stop CM-QS600 in fastboot mode (useful for SW dev)

Power-Down Parallel RGB Shifters

Keep Parallel RGB interface disabled with SB-SOM-QS600 since this interface is not available with CM-QS600 SoM/CoM

VSB_PER_DC
0R R86 — DISPLAYSHIFTER_NOE 5

SB-SOM-QS600 PRIMARY I2C BUS

3,8 P1-69_SPI_CLK — 0R R66 — CARRIER_I2C_SCL_VPER 3,4,9,11,13
3,8 P1-58_SPI_CS0 — 0R R67 — CARRIER_I2C_SDA_VPER 3,4,9,11,13

SB-SOM-QS600 POWER

This enables operation of CM-QS600 from battery
Please note that while CM-QS600 power can be supplied directly from battery, most carrier board components require DC power source to be available for normal operation

VBAT
3,11,15,16 P1-192_RESERVED — R109 0R
C209 100uF

SB-SOM-QS600 GPIO Expander Interrupt

SB-SOM-XXX uses the GPIO function on pin 60 of SoM/CoM interface as an interrupt for SB-SOM-XXX onboard gpio-expander. Using pin 60 with CM-QS600 is not possible since no GPIO is available on CM-QS600 pin 60 under certain conditions (with WB option of SoM).
To overcome this we are using pin 161 of SoM/CoM interface, (which has GPIO functionality with all CM-QS600 configurations), with SB-SOM-QS600

3,8,13 P1-161_GPIO4 — R131 0R — EXPANDER_nINT 4

SB-SOM-QS600 Ethernet LEDs

NOTE: QS600 ethernet controller must be properly configured for ethernet LEDs to operate correctly since default config does not comply with SODIMM204 pinout

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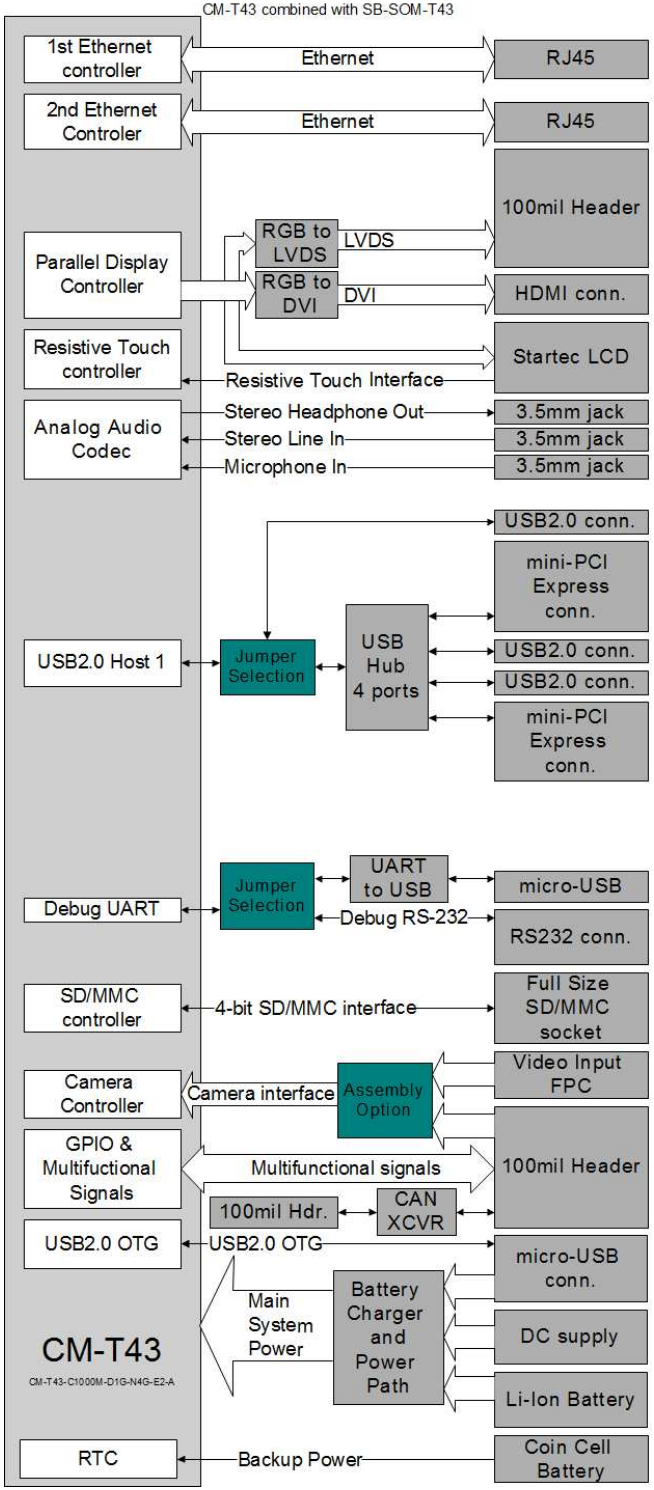
SBC-T43

CM-T43 combined with SB-SOM-T43



SB-SOM-T43 Specific Provisions
Populated only for SB-SOM-T43

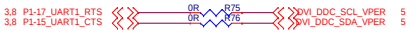
Alternate usage of SATA signals

CM-T43 does not implement the SATA interface.
This provision allows SB-SOM-T43 to route signals otherwise used for SATA, to a 100mil header

SB-SOM-T43 CAN BUS

SB-SOM-T43 PRIMARY DEBUG UART/RS-232

SB-SOM-T43 I2C USED FOR DVI DDC



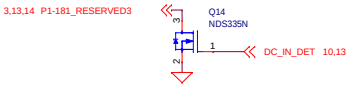
USB1 Host VBUS monitoring

CM-T43 does not implement the BOOT_PWR_IN function on carrier board interface pin 196.
This provision allows CM-T43 to monitor VBUS1 with SB-SOM-T43 board.

SB-SOM-T43 AC POWER & Detection

```
CM-T43 pin 181 = AC_DET

AC_DET Default settings:
1. Pulled to VCC_CM onboard CM-T43
2. Falling edge on AC_DET triggers
transition of CM-T43 from OFF/SUSPED
to WAIT_PWR_EN state.
Normally, CM-T43 then transitions from
WAIT_PWR_EN to ACTIVE state within
20seconds.
```



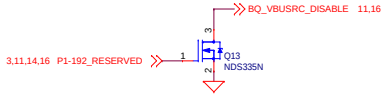
VBUS0 (OTG port) load switch control

CM-T43 can control VBUS0 source (U1 load switch) onboard SB-SOM-T43 through signal on P1-200.
Refer to CM-T43 hardware reference manual for additional details

USB CHARGER LOGIC

CM-T43 drives P1-192_RESERVED
HIGH (3.3V) whenever a USB charger is detected on the device/host USB port
(P3 USB OTG connector, CM-T43 pins 176 & 178).
Please refer to CM-T43 hardware reference manual for additional details

This circuitry makes sure of that if CM-T43 detects a USB charger connected to P3 connector (USB OTG), SB-SOM-T43 can generate VCC_CM (main power rail for CM-T43) from VBUS0 (assuming this rail is the input from the detected charger), allowing the system to be powered from USB power source. Otherwise, assuming VBUS0 is generated onboard SB-SOM-T43, VCC_CM cannot be generated from VBUS0 (preventing reverce power dependency, since in that case VBUS is actually generated from VCC_CM).



CM-T43 2nd ETHERNET ACTIVITY LED

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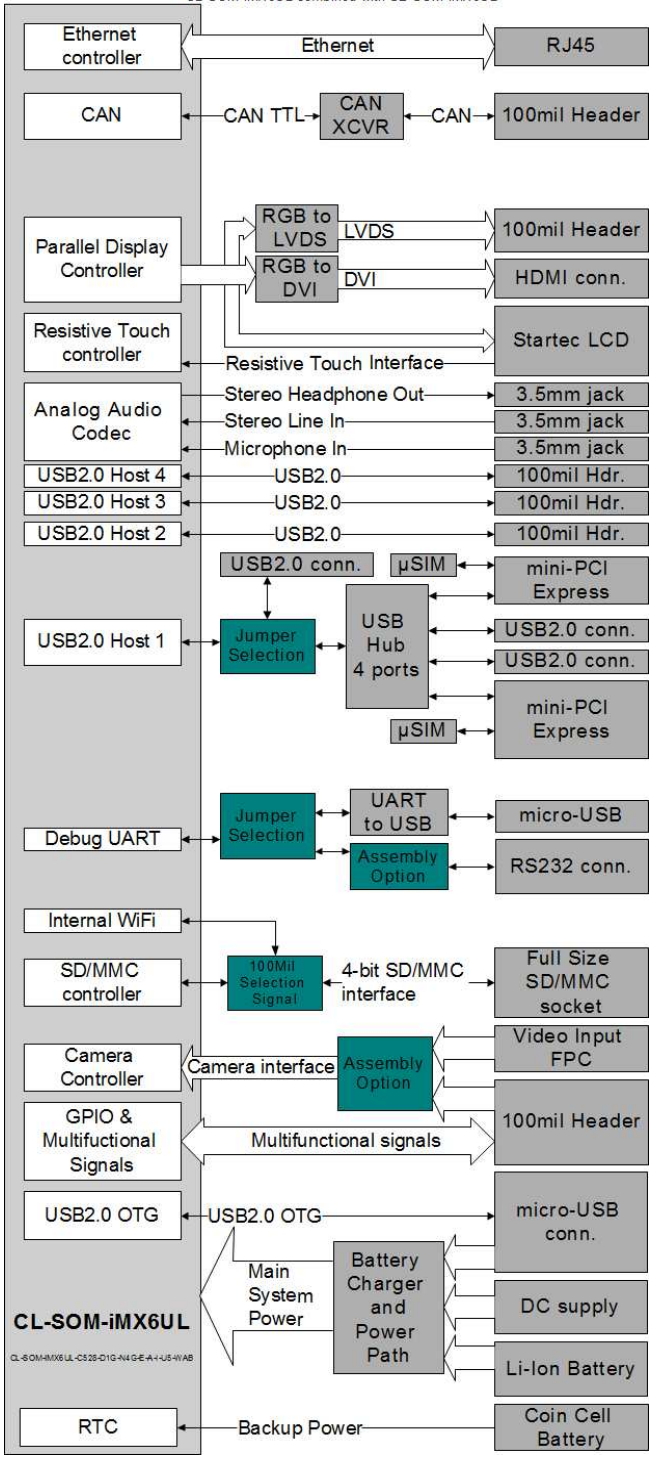
SBC-iMX6UL

CL-SOM-iMX6UL combined with SB-SOM-iMX6UL



SB-SOM-iMX6UL Specific Provisions
Populated only for SB-SOM-iMX6UL

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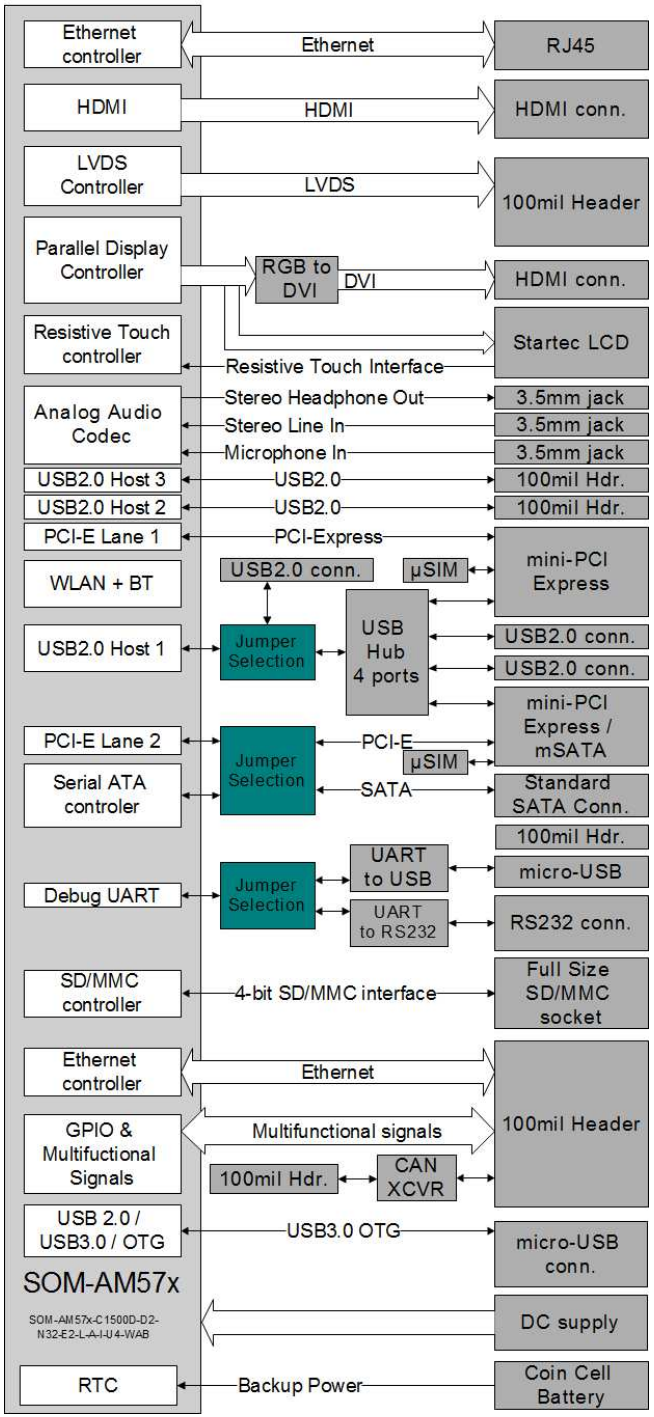
SBC-AM57x

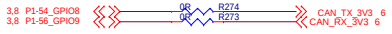
CL-SOM-AM57X combined with SB-SOM-AM57x



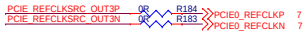
SB-SOM-AM57x Specific Provisions
Populated only for SB-SOM-AM57x

CAN bus

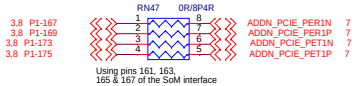
SOM-AM57x DCAN1 interface is exposed through CL-SODIMM pins 54 & 56.



Provision to source PCIE0 REFCLK from GENERATOR to mini-PCI-E connector

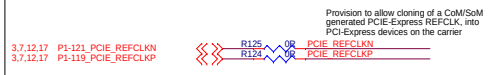


2nd PCI-Express Provision

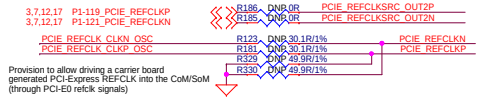


Using pins 161, 163, 165 & 167 of the SoM interface as PCI-Express RX & TX

Provision to drive REFCLK GENERATOR from CoM/SoM sourced PCIE0 REFCLK

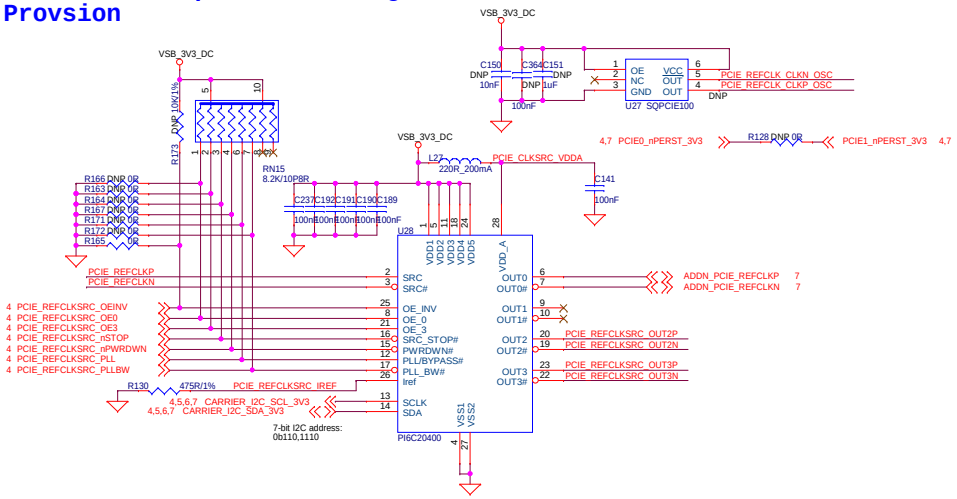


Provision to source generator source REFCLK from onboard source (U27)



Provision to allow driving a carrier board generated PCI-Express REFCLK into the CoM/SoM (through PCI-E0 refclk signals)

SB-SOM PCI-Express REFCLK generator Provsion



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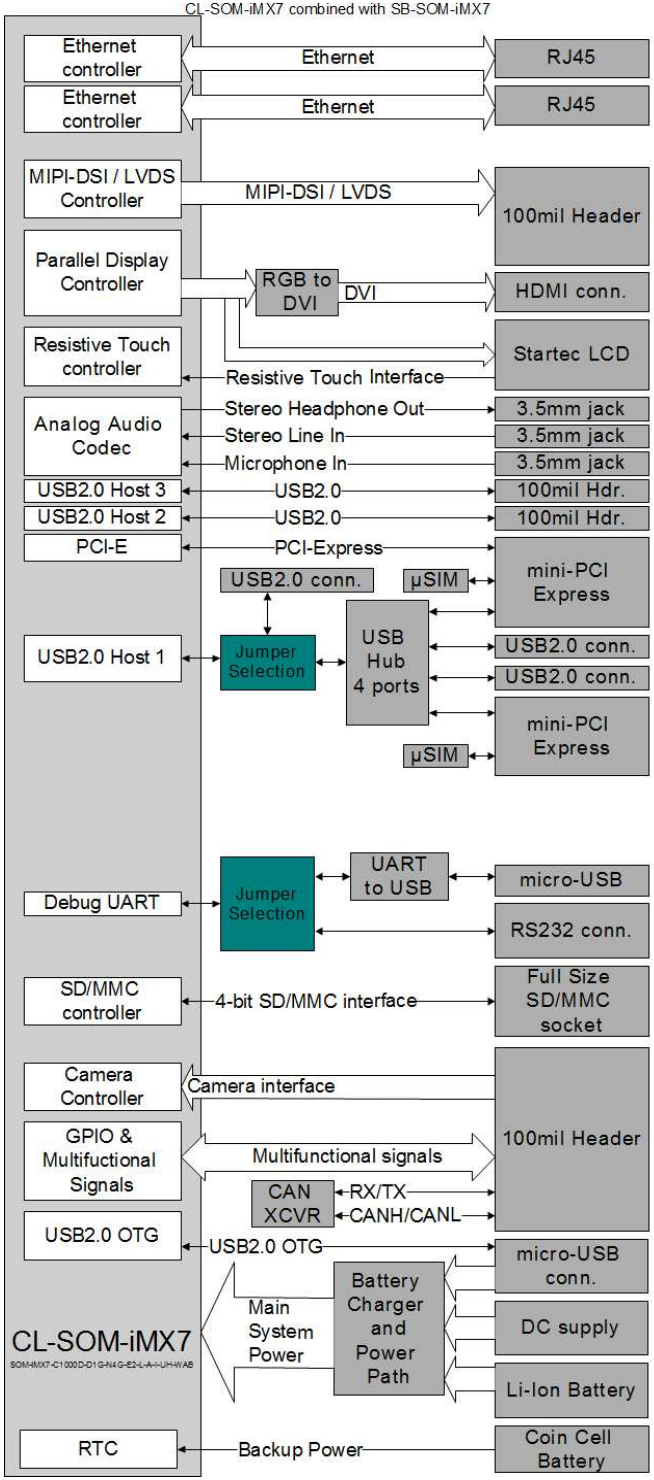
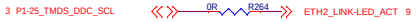
SBC-iMX7

CL-SOM-iMX7 combined with SB-SOM-iMX7

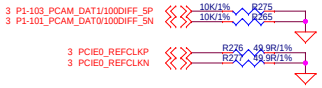


SB-SOM-iMX7 Specific Provisions
Populated only for SB-SOM-iMX7

CL-SOM-iMX7 2nd ETHERNET ACTIVITY LED



CL-SOM-iMX7 PCIe



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